SoC-FPGA Design Guide

Real Time Embedded Systems

LAP – IC – EPFL

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René Beuchat

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# Introduction

The development of embedded systems based on chips containing one or more microprocessors and hardcore peripherals, as well as an FPGA part is becoming more and more important. This technology gives the designer a lot of freedom and powerful abilities. Classical design flows with microcontrollers are emphasized with the full power of FPGAs.

Mixed designs are becoming a reality with. One can now design specific accelerators to greatly improve algorithms, or create specific programmable interfaces with the external world.

Two main HDL (**H**ardware **D**esign **L**anguage) languages are available for the design of the FPGA part: **VHDL** and Verilog. There also exist other tools that perform automatic translations from C to HDL. New emerging technologies like OpenCL allow compatibility between high-level software design, and low-level hardware implementations as:

* Compilation for single or multicore processors
* Compilation for GPUs (Graphical Processing Unit)
* Translation and compilation for FPGAs. The latest models use a PCIe interface or some other way of parameters passing between the main processor and the FPGA

*This guide assumes users know how to use Quartus II, Nios II, Qsys and ModelSim-Altera.*

*All hardware and software examples in this guide were made with “Quartus II”, “SoC EDS” and “Nios II Software Build Tools” version* 14.0*.*

We will be using the Terasic DE1-SoC board: <http://de1-soc.terasic.com>

# Terasic DE1-SoC Board

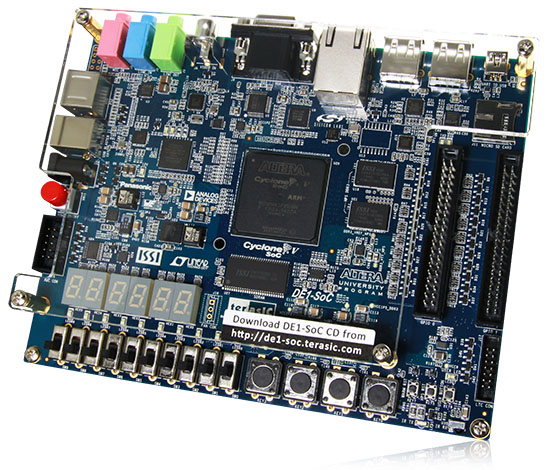


Figure 1. Terasic DE1-SoC Board

The DE1-SoC board has many features that allow users to implement a wide range of designed circuits. We will discuss some noteworthy features in this guide.

## Specifications

### FPGA Device

* Cyclone V SoC 5CSEMA5F31C6 Device
* Dual-core ARM Cortex-A9 (HPS)
* 85K Programmable Logic Elements
* 4’450 Kbits embedded memory
* 6 Fractional PLLs
* 2 Hard Memory Controllers

### Configuration and Debug

* Quad Serial Configuration device – EPCQ256 on FPGA
* On-Board USB Blaster II (Normal type B USB connector)

### Memory Device

* 64 MB (32Mx16) SDRAM on FPGA
* 1 GB (2x256Mx16) DDR3 SDRAM on HPS
* Micro SD Card Socket on HPS

### Communication

* Two Port USB 2.0 Host (ULPI interface with USB type A connector)
* USB to UART (micro USB type B connector)
* 10/100/1000 Ethernet
* PS/2 mouse/keyboard
* IR Emitter/Receiver

### Connectors

* Two 40-pin Expansion Headers
* One 10-pin ADC Input Header
* One LTC connector (One Serial Peripheral Interface (SPI) Master, one I2C and one GPIO interface)

### Display

* 24-bit VGA DAC

### Audio

* 24-bit CODEC, line-in, line-out, and microphone-in jacks

### Video Input

* TV Decoder (NTSC/PAL/SECAM) and TV-in connector

### ADC

* Fast throughput rate: 1 MSPS
* Channel number: 8
* Resolution: 12 bits
* Analog input range : 0 ~ 2.5 V or 0 ~ 5V as selected via the RANGE bit in the control register

### Switches, Buttons and Indicators

* 4 User Keys (FPGA x4)
* 10 User switches (FPGA x10)
* 11 User LEDs (FPGA x10; HPS x 1)
* 2 HPS Reset Buttons (HPS\_RST\_n and HPS\_WARM\_RST\_n)
* Six 7-segment displays

### Sensors

* G-Sensor on HPS

### Power

* 12V DC input

### Block Diagram

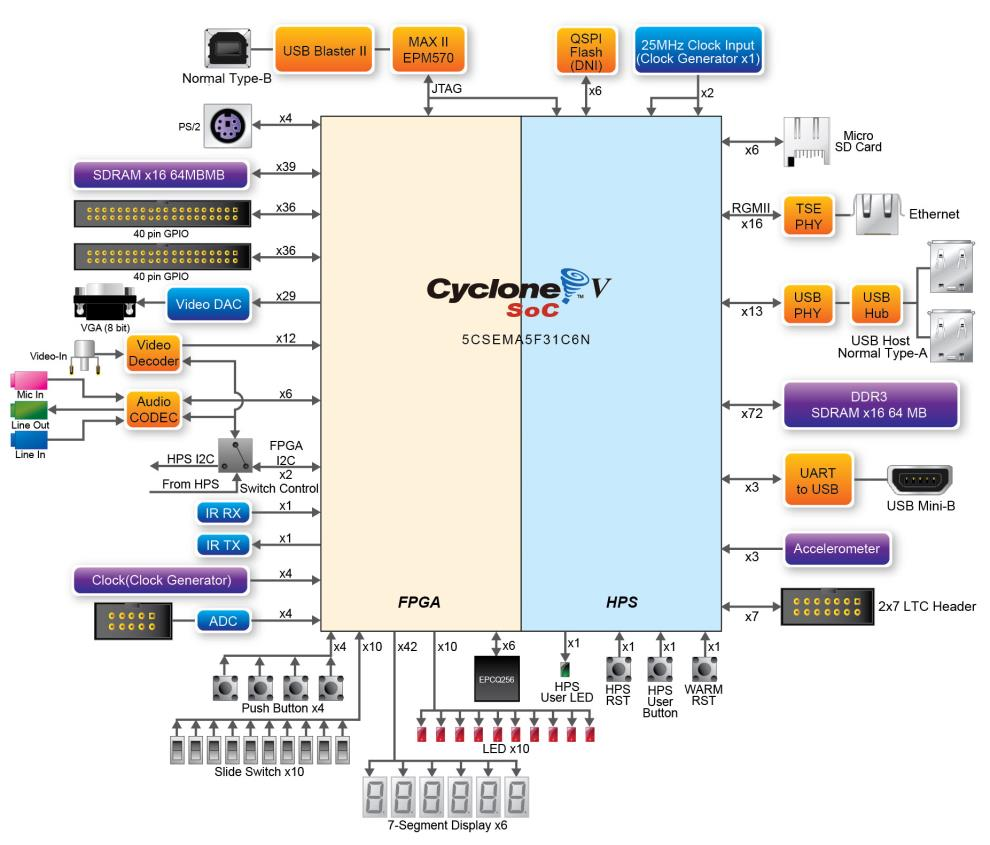


Figure 2. Block Diagram of the DE1-SoC Board

## Layout

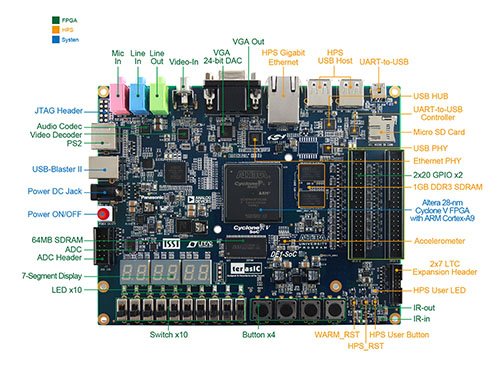


Figure 3. Front

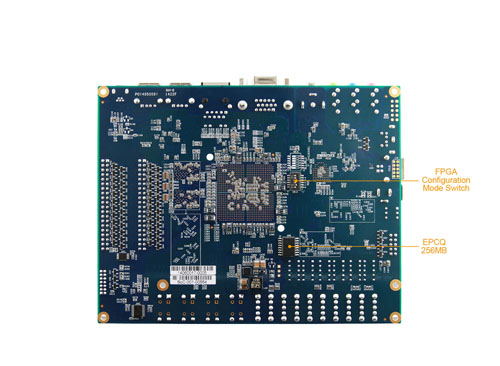


Figure 4. Back

* Green for peripherals directly connected to the FPGA
* Orange for peripherals directly connected to the HPS
* Blue for board control

Manuals and resources are available on the DE1-SoC [resources](http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=165&No=836&PartNo=4ParagrapheTexte) page.

# Cyclone V Overview

This section describes some features of the Cyclone V family of devices. We do not list all features, but only the ones most important to us. All this information, along with the most complete documentation regarding this family can be found on the [Cyclone V Device Handbook](http://www.altera.com/literature/hb/cyclone-v/cyclone5_handbook.pdf), more specifically [Volume 3: Hard Processor System Technical Reference Manual](http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf).

## Introduction to the Cyclone V Hard Processor System

The Cyclone V device is a single-die system on a chip (SoC) that consists of two distinct parts – a hard processor system (HPS) portion and an FPGA portion.



Figure 5. Altera SoC FPGA Device Block Diagram

The HPS contains a microprocessor unit (MPU) subsystem with single or dual ARM Cortex-A9 MPCore processors, flash memory controllers, SDRAM L3 Interconnect, on-chip memories, support peripherals, interface peripherals, debug capabilities, and phase-locked loops (PLLs). The dual-processor HPS supports symmetric (SMP) and asymmetric (AMP) multiprocessing.

The DE1-SoC has a dual-processor HPS.

The FPGA portion of the device contains the FPGA fabric, a control block (CB), phase-locked loops (PLLs), and depending on the device variant, high-speed serial interface (HSSI) transceivers, hard PCI Express (PCIe) controllers, and hard memory controllers.

The DE1-SoC does not contain any HSSI transceivers, or hard PCIe controllers.

The HPS and FPGA portions of the device are distinctly different. The HPS can boot from multiple sources, including the FPGA fabric and external flash. In contrast, the FPGA must be configured through either the HPS or an externally supported device.

The MPU subsystem can boot from flash devices connected to the HPS pins. Or, when the FPGA portion is configured by an external source, the MPU subsystem can boot from memory available on the FPGA portion of the device.

The HPS and FPGA portions of the device each have their own pins. Pins are not freely shared between the HPS and the FPGA fabric. The FPGA I/O pins are configured by an FPGA configuration image through the HPS or any external source supported by the device. The HPS I/O pins are configured by software executing in the HPS. Software executing on the HPS accesses control registers in the system manager to assign HPS I/O pins to the available HPS modules.

The software that configures the HPS I/O pins is called the Preloader.

The HPS and FPGA portions of the device have separate external power supplies and independently power on. You can power on the HPS without powering on the FPGA portion of the device. However, to power on the FPGA portion, the HPS must already be on or powered on at the same time as the FPGA portion. You can also turn off the FPGA portion of the device while leaving the HPS power on.

## Features of the HPS



Figure 6. HPS Block Diagram

The following list contains the main modules of the HPS:

* MPU subsystem featuring dual ARM Cortex-A9 MPCore processors
* General-purpose Direct Memory Access (DMA) controller
* Two Ethernet media access controllers (EMACs)
* Two USB 2.0 On-The-Go (OTG) controllers
* NAND flash controller
* Quad SPI flash controller
* Secure Digital (SD) / MultiMediaCard (MMC) controller
* Two serial peripheral interface (SPI) master controllers
* Two SPI slave controllers
* Four inter-integrated circuit (I2C) controllers
* 64 KB on-chip RAM
* 64 KB on-chip boot ROM
* Two UARTs
* Four timers
* Two watchdog timers
* Three general-purpose I/O (GPIO) interfaces
* Two controller area network (CAN) controllers
* ARM CoreSight debug components
* System manager
* Clock manager
* Reset manager
* Scan manager
* FPGA manager

## System Integration Overview

In this part, we briefly go through some features provided by the most important HPS components.

### MPU Subsystem

Here are a few important features of the MPU subsystem:

* Interrupt controller
* One general-purpose timer and one watchdog timer per processor
* One Memory management unit (MMU) per processor

The HPS masters the L3 interconnect and the SDRAM controller subsystem.

### SDRAM Controller Subsystem

The SDRAM controller subsystem is mastered by HPS masters and FPGA fabric masters. It supports DDR2, DDR3, and LPDDR2 devices. It is composed of 2 parts:

* SDRAM controller
* DDR PHY (interfaces the single port memory controller to the HPS I/O)

The DE1-SoC contains DDR3 SDRAM on the HPS

### Support Peripherals

#### System Manager

This is one of the most essential HPS components. It offers a few important features:

* Pin multiplexing (term used for the software configuration of the HPS I/O pins by the Preloader)
* Freeze controller that places I/O elements into a safe state for configuration
* Low-level control of peripheral features not accessible through the control and status registers (CSRs)

The low-level control of some peripheral features that are not accessible through the CSRs is not externally documented. You will see this type of code when you generate your custom preloader, but must not use the constructs in your own code.

#### FPGA Manager

The FPGA manager offers the following features:

* Manages configuration of the FPGA portion of the device
* Monitors configuration-related signals in the FPGA
* Provides 32 general-purpose inputs and 32 general-purpose outputs to the FPGA fabric

### Interface Peripherals

#### GPIO Interfaces

The HPS provides three GPIO interfaces and offer the following features:

* Supports digital de-bounce
* Configurable interrupt mode
* Supports up to 71 I/O pins and 14 input-only pins, based on device variant
* Supports up to 67 I/O pins and 14 input-only pins

The DE1-SoC has 67 I/O pins and 14 input-only pins

### On-Chip Memory

The following on-chip memories are different from any on-chip memories located in the FPGA fabric.

#### On-Chip RAM

The on-chip RAM offers the following features:

* 64 KB size
* High performance for all burst lengths

#### Boot ROM

The boot ROM offers the following features:

* 64 KB size
* Contains the code required to support HPS boot from cold or warm reset
* Used exclusively for booting the HPS

The code in the boot ROM cannot be changed.

## HPS-FPGA Interfaces

The HPS-FPGA interfaces provide a variety of communication channels between the HPS and the FPGA fabric. The HPS-FPGA interfaces include:

* FPGA-to-HPS bridge – a high performance bus with a configurable data width of 32, 64, or 128 bits. It allows the FPGA fabric to master transactions to slaves in the HPS. This interface allows the FPGA fabric to have full visibility into the HPS address space.
* HPS-to-FPGA bridge – a high performance bus with a configurable data width of 32, 64, or 128 bits. It allows the HPS to master transactions to slaves in the FPGA fabric. I will sometimes call this the “heavyweight” HPS-to-FPGA bridge to distinguish its “lightweight” counterpart (see below).
* Lightweight HPS-to-FPGA bridge – a bus with a 32-bit fixed data width. It allows the HPS to master transactions to slaves in the FPGA fabric.
* FPGA manager interface – signals that communicate with FPGA fabric for boot and configuration.
* Interrupts – allow soft IP to supply interrupts directly to the MPU interrupt controller.
* HPS debug interface – an interface that allows the HPS debug control domain to extend into the FPGA.

## HPS Address Map

### HPS Address Spaces

The HPS address map specifies the address of slaves, such as memory and peripherals, as viewed by the HPS masters. The HPS has 3 address spaces:

|  |  |  |
| --- | --- | --- |
| Name | Description | Size |
| MPU | MPU subsystem | 4 GB |
| L3 | L3 interconnect | 4 GB |
| SDRAM | SDRAM controller subsystem | 4 GB |

Table 1. HPS Address Spaces

The following figure shows the relationships between the different HPS address spaces. The figure is not to scale.



Figure 7. HPS Address Space Relations

The window regions provide access to other address spaces. The thin black arrows indicate which address space is accessed by a window region (arrows point to accessed address space).

The SDRAM window in the MPU can grow and shrink at the top and bottom (short blue vertical arrows) at the expense of the FPGA slaves and boot regions. The ACP window can be mapped to any 1 GB region in the MPU address space (blue vertical bidirectional arrow), on gigabyte-aligned boundaries.

The following table shows the base address and size of each region that is common to the L3 and MPU address spaces.

|  |  |  |  |
| --- | --- | --- | --- |
| Region Name | Description | Base Address | Size |
| FPGA slaves | FPGA slaves connected to the HPS-to-FPGA bridge | 0xC0000000 | 960 MB |
| HPS peripherals | Slaves directly connected to the HPS (corresponds to all orange colored elements on Figure 3 and Figure 4) | 0xFC000000 | 64 MB |
| Lightweight FPGA slaves | FPGA slaves connected to the lightweight HPS-to-FPGA bridge | 0xFF200000 | 2 MB |

Table 2. Common Address Space Regions

### HPS Peripheral Region Address Map

The following table lists the slave identifier, slave title, base address, and size of each slave in the HPS peripheral region. The Slave Identifier column lists the names used in the HPS register map file provided by Altera (more on this later).

|  |  |  |  |
| --- | --- | --- | --- |
| Slave Identifier | Slave Title | Base Address | Size |
| STM | STM | 0xFC000000 | 48 MB |
| DAP | DAP | 0xFF000000 | 2 MB |
| LWFPGASLAVES | FPGA slaves accessed with lightweight HPS-to-FPGA bridge | 0xFF200000 | 2 MB |
| LWHPS2FPGAREGS | Lightweight HPS-to-FPGA bridge GPV | 0xFF400000 | 1 MB |
| HPS2FPGAREGS | HPS-to-FPGA bridge GPV | 0xFF500000 | 1 MB |
| FPGA2HPSREGS | FPGA-to-HPS bridge GPV | 0xFF600000 | 1 MB |
| EMAC0 | EMAC0 | 0xFF700000 | 8 KB |
| EMAC1 | EMAC1 | 0xFF702000 | 8 KB |
| SDMMC | SD/MMC | 0xFF704000 | 4 KB |
| QSPIREGS | Quad SPI flash controller registers | 0xFF705000 | 4 KB |
| FPGAMGRREGS | FPGA manager registers | 0xFF706000 | 4 KB |
| ACPIDMAP | ACP ID mapper registers | 0xFF707000 | 4 KB |
| GPIO0 | GPIO0 | 0xFF708000 | 4 KB |
| GPIO1 | GPIO1 | 0xFF709000 | 4 KB |
| GPIO2 | GPIO2 | 0xFF70A000 | 4 KB |
| L3REGS | L3 interconnect GPV | 0xFF800000 | 1 MB |
| NANDDATA | NAND controller data | 0xFF900000 | 1 MB |
| QSPIDATA | Quad SPI flash data | 0xFFA00000 | 1 MB |
| USB0 | USB0 OTG controller registers | 0xFFB00000 | 256 KB |
| USB1 | USB1 OTG controller registers | 0xFFB40000 | 256 KB |
| NANDREGS | NAND controller registers | 0xFFB80000 | 64 KB |
| FPGAMGRDATA | FPGA manager configuration data | 0xFFB90000 | 4 KB |
| CAN0 | CAN0 controller registers | 0xFFC00000 | 4 KB |
| CAN1 | CAN1 controller registers | 0xFFC01000 | 4 KB |
| UART0 | UART0 | 0xFFC02000 | 4 KB |
| UART1 | UART1 | 0xFFC03000 | 4 KB |
| I2C0 | I2C0 | 0xFFC04000 | 4 KB |
| I2C1 | I2C1 | 0xFFC05000 | 4 KB |
| I2C2 | I2C2 | 0xFFC06000 | 4 KB |
| I2C3 | I2C3 | 0xFFC07000 | 4 KB |
| SPTIMER0 | SP Timer0 | 0xFFC08000 | 4 KB |
| SPTIMER1 | SP Timer1 | 0xFFC09000 | 4 KB |
| SDRREGS | SDRAM controller subsystem registers | 0xFFC20000 | 128 KB |
| OSC1TIMER0 | OSC1 Timer0 | 0xFFD00000 | 4 KB |
| OSC1TIMER1 | OSC1 Timer1 | 0xFFD01000 | 4 KB |
| L4WD0 | Watchdog0 | 0xFFD02000 | 4 KB |
| L4WD1 | Watchdog1 | 0xFFD03000 | 4 KB |
| CLKMGR | Clock manager | 0xFFD04000 | 4 KB |
| RSTMGR | Reset manager | 0xFFD05000 | 4 KB |
| SYSMGR | System manager | 0xFFD08000 | 16 KB |
| DMANONSECURE | DMA nonsecure registers | 0xFFE00000 | 4 KB |
| DMASECURE | DMA secure registers | 0xFFE01000 | 4 KB |
| SPIS0 | SPI slave0 | 0xFFE02000 | 4 KB |
| SPIS1 | SPI slave1 | 0xFFE03000 | 4 KB |
| SPIM0 | SPI master0 | 0xFFF00000 | 4 KB |
| SPIM1 | SPI master1 | 0xFFF01000 | 4 KB |
| SCANMGR | Scan manager registers | 0xFFF02000 | 4 KB |
| ROM | Boot ROM | 0xFFFD0000 | 64 KB |
| MPUSCU | MPU SCU registers | 0xFFFEC000 | 8 KB |
| MPUL2 | MPU L2 cache controller registers | 0xFFFEF000 | 4 KB |
| OCRAM | On-chip RAM | 0xFFFF0000 | 64 KB |

Table 3. HPS Peripheral Region Address Map

The programming model for accessing the HPS peripherals in Table 3 is the same as for peripherals created on the FPGA fabric. That is, every peripheral has a base address at which a certain number of registers can be found. You then read and write to a certain set of these registers in order to modify the peripheral’s behavior.

You do not need to hard-code any base addresses or peripheral register maps in your programs, as Altera provides a header file for each HPS peripheral in Table 3.

Two directories contain all HPS-related header files:

1. “<altera\_install\_directory>\embedded\ip\altera\hps\altera\_hps\hwlib\include”

Contains high-level header files that typically contain a few functions which facilitate control over the HPS components.

1. “<altera\_install\_directory>\embedded\ip\altera\hps\altera\_hps\hwlib\include\socal”

Contains low-level header files that provide a peripheral’s bit-level register details. For example, any bits in a peripheral’s register that correspond to undefined behavior will be specified in these header files.

To illustrate the differences among the high and low-level header files, we can compare the ones related to the FPGA manager peripheral:

1. “…\hwlib\include\alt\_fpga\_manager.h”

ALT\_STATUS\_CODE alt\_fpga\_reset\_assert(void);

ALT\_STATUS\_CODE alt\_fpga\_configure(const void\* cfg\_buf, size\_t cfg\_buf\_len);

1. “…\hwlib\include\socal\alt\_fpgamgr.h”

/\* The width in bits of the ALT\_FPGAMGR\_CTL\_EN register field. \*/

#define ALT\_FPGAMGR\_CTL\_EN\_WIDTH 1

/\* The mask used to set the ALT\_FPGAMGR\_CTL\_EN register field value. \*/

#define ALT\_FPGAMGR\_CTL\_EN\_SET\_MSK 0x00000001

/\* The mask used to clear the ALT\_FPGAMGR\_CTL\_EN register field value. \*/

#define ALT\_FPGAMGR\_CTL\_EN\_CLR\_MSK 0xfffffffe

An important header file is “…\hwlib\include\socal\hps.h”. It contains the HPS component’s full register map, as provided in Table 3. Note however, that there exists no header file for the “heavyweight” HPS-to-FPGA bridge, as it is not located in the “HPS peripherals” region in Figure 7. Indeed, the “heavyweight” HPS-to-FPGA bridge is not considered a HPS peripheral, whereas the lightweight HPS-to-FPGA bridge is.

Therefore, in order to use the “heavyweight” HPS-to-FPGA bridge, you will have to define a macro in your code, as follows:

#define ALT\_HWFPGASLVS\_OFST 0xc0000000

The reason why the “lightweight” HPS-to-FPGA bridge is considered a HPS peripheral may be related to the fact that it has a fixed 32-bit bus width (coincidence that this corresponds to the HPS’ native data size?)

## HPS Booting and FPGA Configuration

Before being able to use the Cyclone V SoC, one needs to understand how the HPS boots and how the FPGA can be configured.

### HPS Booting



Figure 8. HPS Boot Flows

Booting software on the HPS is a multi-stage process. Each stage is responsible for loading the next stage. The first software stage is the boot ROM. The boot ROM code locates and executes the second software stage, called the preloader. The preloader locates, and if present, executes the next software stage. The preloader and subsequent software stages are collectively referred to as user software.

The reset, boot ROM, and preloader stages are always present in the HPS boot flow. The subsequent stage(s) that comes after the preloader depends on the type of application you want to run. The HPS can execute 2 types of applications:

* Bare-metal applications (no operating system)
* Applications on top of an operating system (Linux)

Figure 8 shows the HPS’ available boot flows. The Reset and Boot ROM stages are the only fixed parts of the boot process. Everything in the user software stages can be customized.

Although the DE1-SoC has a dual-processor HPS, CPU1 is under reset, and the boot flow only executes on CPU0. User software executing on CPU0 is responsible to release CPU1 from reset.

#### HPS State on Entry to the Preloader

When the boot ROM code is ready to pass control to the preloader, the processor (CPU0) is in the following state:

* Instruction cache is enabled
* Branch predictor is enabled
* Data cache is disabled
* MMU is disabled
* Floating point unit is enabled
* NEON vector unit is enabled
* Processor is in ARM secure supervisor mode
* The L4 watchdog 0 timer is active and has been toggled

#### Preloader

The preloader is the most important of all boot stages. It is actually what one would call the boot “source”, as all stages before it are unmodifiable. Although all stages of the User Software box in Figure 8 can be customized, the preloader is typically the only one that is. It can be stored on external flash-based memory, or in the FPGA fabric.

The following list shows the various HPS boot sources:

* NAND flash memory through the NAND flash controller
* SD/MMC flash memory through the SD/MMC flash controller
* SPI and QSPI flash memory through the QSPI flash controller using Slave Select 0
* FPGA fabric on-chip memory

The DE1-SoC can only boot from SD/MMC flash memory. Although its HPS contains all necessary controllers, the board doesn’t have a DIP switch to choose the boot source among those listed above. This DIP switch, if present, modifies the BOOTSEL and CLKSEL values which the boot ROM uses to select the boot source. The physical location of the DIP switch is present underneath the board, but a switch isn’t soldered.

Depending of the boot device, the preloader’s execution can be either direct, or indirect:

* With indirect execution, the boot ROM code copies the preloader from the boot device to the HPS on-chip RAM and jumps to it. Indirect execution is used for flash memory boot sources.
* With direct execution, the boot ROM code jumps to the preloader located in the FPGA fabric.

The preloader typically performs the following actions:

* Initialize the SDRAM interface
* Configure the HPS I/O through the scan manager
* Configure pin multiplexing through the system manager
* Configure HPS clocks through the clock manager
* Initialize the flash controller (NAND, SD/MMC, QSPI) that contains the next stage boot software
* Load the next boot software into the SDRAM and pass control to it

The preloader does not release CPU1 from reset. The subsequent stages of the boot process are responsible for it if they want to use the extra processor.

# Using the Cyclone V

## Hardware

The HPS component is a soft component, but it does not mean that the HPS is a softcore processor. In fact, the HPS exclusively contains hard logic. The reason it is considered a softcore component originates from the fact that it enables other soft components to interface with the HPS hard logic. As such, the HPS component has a small footprint in the FPGA fabric, as its only purpose is to connect the soft and hard logic together.

Therefore, it is possible to use the Cyclone V SoC in 3 different configurations:

* FPGA-only
* HPS-only
* HPS & FPGA

We will look at these different configurations below. The configurations using the HPS are more difficult to configure than the FPGA-only one.

### FPGA-only

Exclusively using the FPGA part of the Cyclone V is easy, as the design process is identical to any other Altera FPGA. The only software needed is Quartus II. You can build a complete design, then program the FPGA through the Quartus II Programmer.

#### DE1-SoC Top-level VHDL Entity

The DE1-SoC has a lot of pins, which makes it tedious to start an FPGA design. I recommend using the following entity for your top-level VHDL file, as it contains all the board’s FPGA and HPS pins:

entity de1\_soc is

port (

-- ADC

ADC\_CS\_n : out std\_logic;

ADC\_DIN : out std\_logic;

ADC\_DOUT : in std\_logic;

ADC\_SCLK : out std\_logic;

-- Audio

AUD\_ADCDAT : in std\_logic;

AUD\_ADCLRCK : inout std\_logic;

AUD\_BCLK : inout std\_logic;

AUD\_DACDAT : out std\_logic;

AUD\_DACLRCK : inout std\_logic;

AUD\_XCK : out std\_logic;

-- CLOCK

CLOCK\_50 : in std\_logic;

CLOCK2\_50 : in std\_logic;

CLOCK3\_50 : in std\_logic;

CLOCK4\_50 : in std\_logic;

-- SDRAM

DRAM\_ADDR : out std\_logic\_vector(12 downto 0);

DRAM\_BA : out std\_logic\_vector(1 downto 0);

DRAM\_CAS\_N : out std\_logic;

DRAM\_CKE : out std\_logic;

DRAM\_CLK : out std\_logic;

DRAM\_CS\_N : out std\_logic;

DRAM\_DQ : inout std\_logic\_vector(15 downto 0);

DRAM\_LDQM : out std\_logic;

DRAM\_RAS\_N : out std\_logic;

DRAM\_UDQM : out std\_logic;

DRAM\_WE\_N : out std\_logic;

-- I2C for Audio and Video-In

FPGA\_I2C\_SCLK : out std\_logic;

FPGA\_I2C\_SDAT : inout std\_logic;

-- SEG7

HEX0 : out std\_logic\_vector(6 downto 0);

HEX1 : out std\_logic\_vector(6 downto 0);

HEX2 : out std\_logic\_vector(6 downto 0);

HEX3 : out std\_logic\_vector(6 downto 0);

HEX4 : out std\_logic\_vector(6 downto 0);

HEX5 : out std\_logic\_vector(6 downto 0);

-- IR

IRDA\_RXD : in std\_logic;

IRDA\_TXD : out std\_logic;

-- KEY

KEY : in std\_logic\_vector(3 downto 0);

-- LED

LEDR : out std\_logic\_vector(9 downto 0);

-- PS2

PS2\_CLK : inout std\_logic;

PS2\_CLK2 : inout std\_logic;

PS2\_DAT : inout std\_logic;

PS2\_DAT2 : inout std\_logic;

-- SW

SW : in std\_logic\_vector(9 downto 0);

-- Video-In

TD\_CLK27 : inout std\_logic;

TD\_DATA : out std\_logic\_vector(7 downto 0);

TD\_HS : out std\_logic;

TD\_RESET\_N : out std\_logic;

TD\_VS : out std\_logic;

-- VGA

VGA\_B : out std\_logic\_vector(7 downto 0);

VGA\_BLANK\_N : out std\_logic;

VGA\_CLK : out std\_logic;

VGA\_G : out std\_logic\_vector(7 downto 0);

VGA\_HS : out std\_logic;

VGA\_R : out std\_logic\_vector(7 downto 0);

VGA\_SYNC\_N : out std\_logic;

VGA\_VS : out std\_logic;

-- GPIO\_0, GPIO\_0 connect to GPIO Default

GPIO\_0 : inout std\_logic\_vector(35 downto 0);

-- GPIO\_1, GPIO\_1 connect to GPIO Default

GPIO\_1 : inout std\_logic\_vector(35 downto 0);

-- HPS

HPS\_CONV\_USB\_N : inout std\_logic;

HPS\_DDR3\_ADDR : out std\_logic\_vector(14 downto 0);

HPS\_DDR3\_BA : out std\_logic\_vector(2 downto 0);

HPS\_DDR3\_CAS\_N : out std\_logic;

HPS\_DDR3\_CK\_N : out std\_logic;

HPS\_DDR3\_CK\_P : out std\_logic;

HPS\_DDR3\_CKE : out std\_logic;

HPS\_DDR3\_CS\_N : out std\_logic;

HPS\_DDR3\_DM : out std\_logic\_vector(3 downto 0);

HPS\_DDR3\_DQ : inout std\_logic\_vector(31 downto 0);

HPS\_DDR3\_DQS\_N : inout std\_logic\_vector(3 downto 0);

HPS\_DDR3\_DQS\_P : inout std\_logic\_vector(3 downto 0);

HPS\_DDR3\_ODT : out std\_logic;

HPS\_DDR3\_RAS\_N : out std\_logic;

HPS\_DDR3\_RESET\_N : out std\_logic;

HPS\_DDR3\_RZQ : in std\_logic;

HPS\_DDR3\_WE\_N : out std\_logic;

HPS\_ENET\_GTX\_CLK : out std\_logic;

HPS\_ENET\_INT\_N : inout std\_logic;

HPS\_ENET\_MDC : out std\_logic;

HPS\_ENET\_MDIO : inout std\_logic;

HPS\_ENET\_RX\_CLK : in std\_logic;

HPS\_ENET\_RX\_DATA : in std\_logic\_vector(3 downto 0);

HPS\_ENET\_RX\_DV : in std\_logic;

HPS\_ENET\_TX\_DATA : out std\_logic\_vector(3 downto 0);

HPS\_ENET\_TX\_EN : out std\_logic;

HPS\_FLASH\_DATA : inout std\_logic\_vector(3 downto 0);

HPS\_FLASH\_DCLK : out std\_logic;

HPS\_FLASH\_NCSO : out std\_logic;

HPS\_GPIO : inout std\_logic\_vector(1 downto 0);

HPS\_GSENSOR\_INT : inout std\_logic;

HPS\_I2C\_CONTROL : inout std\_logic;

HPS\_I2C1\_SCLK : inout std\_logic;

HPS\_I2C1\_SDAT : inout std\_logic;

HPS\_I2C2\_SCLK : inout std\_logic;

HPS\_I2C2\_SDAT : inout std\_logic;

HPS\_KEY : inout std\_logic;

HPS\_LED : inout std\_logic;

HPS\_SD\_CLK : out std\_logic;

HPS\_SD\_CMD : inout std\_logic;

HPS\_SD\_DATA : inout std\_logic\_vector(3 downto 0);

HPS\_SPIM\_CLK : out std\_logic;

HPS\_SPIM\_MISO : in std\_logic;

HPS\_SPIM\_MOSI : out std\_logic;

HPS\_SPIM\_SS : inout std\_logic;

HPS\_UART\_RX : in std\_logic;

HPS\_UART\_TX : out std\_logic;

HPS\_USB\_CLKOUT : in std\_logic;

HPS\_USB\_DATA : inout std\_logic\_vector(7 downto 0);

HPS\_USB\_DIR : in std\_logic;

HPS\_USB\_NXT : in std\_logic;

HPS\_USB\_STP : out std\_logic

);

end entity de1\_soc;

Figure 9. DE1-SoC Top-level VHDL Entity

#### DE1-SoC Pin Assignment TCL script

In addition to the entity above, I recommend using the following TCL script in Quartus II to specify the board’s device ID and all its pin assignments:

set\_global\_assignment -name FAMILY "Cyclone V"

set\_global\_assignment -name DEVICE 5CSEMA5F31C6

set\_global\_assignment -name DEVICE\_FILTER\_PACKAGE FBGA

set\_global\_assignment -name DEVICE\_FILTER\_PIN\_COUNT 896

set\_global\_assignment -name DEVICE\_FILTER\_SPEED\_GRADE 6

#============================================================

# ADC

#============================================================

set\_location\_assignment PIN\_AJ4 -to ADC\_CS\_N

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to ADC\_CS\_N

set\_location\_assignment PIN\_AK4 -to ADC\_DIN

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to ADC\_DIN

set\_location\_assignment PIN\_AK3 -to ADC\_DOUT

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to ADC\_DOUT

set\_location\_assignment PIN\_AK2 -to ADC\_SCLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to ADC\_SCLK

#============================================================

# Audio

#============================================================

set\_location\_assignment PIN\_K7 -to AUD\_ADCDAT

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to AUD\_ADCDAT

set\_location\_assignment PIN\_K8 -to AUD\_ADCLRCK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to AUD\_ADCLRCK

set\_location\_assignment PIN\_H7 -to AUD\_BCLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to AUD\_BCLK

set\_location\_assignment PIN\_J7 -to AUD\_DACDAT

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to AUD\_DACDAT

set\_location\_assignment PIN\_H8 -to AUD\_DACLRCK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to AUD\_DACLRCK

set\_location\_assignment PIN\_G7 -to AUD\_XCK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to AUD\_XCK

#============================================================

# CLOCK

#============================================================

set\_location\_assignment PIN\_AF14 -to CLOCK\_50

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to CLOCK\_50

set\_location\_assignment PIN\_AA16 -to CLOCK2\_50

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to CLOCK2\_50

set\_location\_assignment PIN\_Y26 -to CLOCK3\_50

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to CLOCK3\_50

set\_location\_assignment PIN\_K14 -to CLOCK4\_50

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to CLOCK4\_50

#============================================================

# SDRAM

#============================================================

set\_location\_assignment PIN\_AK14 -to DRAM\_ADDR[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[0]

set\_location\_assignment PIN\_AH14 -to DRAM\_ADDR[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[1]

set\_location\_assignment PIN\_AG15 -to DRAM\_ADDR[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[2]

set\_location\_assignment PIN\_AE14 -to DRAM\_ADDR[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[3]

set\_location\_assignment PIN\_AB15 -to DRAM\_ADDR[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[4]

set\_location\_assignment PIN\_AC14 -to DRAM\_ADDR[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[5]

set\_location\_assignment PIN\_AD14 -to DRAM\_ADDR[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[6]

set\_location\_assignment PIN\_AF15 -to DRAM\_ADDR[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[7]

set\_location\_assignment PIN\_AH15 -to DRAM\_ADDR[8]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[8]

set\_location\_assignment PIN\_AG13 -to DRAM\_ADDR[9]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[9]

set\_location\_assignment PIN\_AG12 -to DRAM\_ADDR[10]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[10]

set\_location\_assignment PIN\_AH13 -to DRAM\_ADDR[11]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[11]

set\_location\_assignment PIN\_AJ14 -to DRAM\_ADDR[12]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_ADDR[12]

set\_location\_assignment PIN\_AF13 -to DRAM\_BA[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_BA[0]

set\_location\_assignment PIN\_AJ12 -to DRAM\_BA[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_BA[1]

set\_location\_assignment PIN\_AF11 -to DRAM\_CAS\_N

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_CAS\_N

set\_location\_assignment PIN\_AK13 -to DRAM\_CKE

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_CKE

set\_location\_assignment PIN\_AG11 -to DRAM\_CS\_N

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_CS\_N

set\_location\_assignment PIN\_AH12 -to DRAM\_CLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_CLK

set\_location\_assignment PIN\_AK6 -to DRAM\_DQ[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[0]

set\_location\_assignment PIN\_AJ7 -to DRAM\_DQ[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[1]

set\_location\_assignment PIN\_AK7 -to DRAM\_DQ[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[2]

set\_location\_assignment PIN\_AK8 -to DRAM\_DQ[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[3]

set\_location\_assignment PIN\_AK9 -to DRAM\_DQ[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[4]

set\_location\_assignment PIN\_AG10 -to DRAM\_DQ[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[5]

set\_location\_assignment PIN\_AK11 -to DRAM\_DQ[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[6]

set\_location\_assignment PIN\_AJ11 -to DRAM\_DQ[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[7]

set\_location\_assignment PIN\_AH10 -to DRAM\_DQ[8]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[8]

set\_location\_assignment PIN\_AJ10 -to DRAM\_DQ[9]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[9]

set\_location\_assignment PIN\_AJ9 -to DRAM\_DQ[10]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[10]

set\_location\_assignment PIN\_AH9 -to DRAM\_DQ[11]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[11]

set\_location\_assignment PIN\_AH8 -to DRAM\_DQ[12]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[12]

set\_location\_assignment PIN\_AH7 -to DRAM\_DQ[13]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[13]

set\_location\_assignment PIN\_AJ6 -to DRAM\_DQ[14]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[14]

set\_location\_assignment PIN\_AJ5 -to DRAM\_DQ[15]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_DQ[15]

set\_location\_assignment PIN\_AB13 -to DRAM\_LDQM

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_LDQM

set\_location\_assignment PIN\_AE13 -to DRAM\_RAS\_N

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_RAS\_N

set\_location\_assignment PIN\_AK12 -to DRAM\_UDQM

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_UDQM

set\_location\_assignment PIN\_AA13 -to DRAM\_WE\_N

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to DRAM\_WE\_N

#============================================================

# I2C for Audio and Video-In

#============================================================

set\_location\_assignment PIN\_J12 -to FPGA\_I2C\_SCLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to FPGA\_I2C\_SCLK

set\_location\_assignment PIN\_K12 -to FPGA\_I2C\_SDAT

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to FPGA\_I2C\_SDAT

#============================================================

# SEG7

#============================================================

set\_location\_assignment PIN\_AE26 -to HEX0[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX0[0]

set\_location\_assignment PIN\_AE27 -to HEX0[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX0[1]

set\_location\_assignment PIN\_AE28 -to HEX0[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX0[2]

set\_location\_assignment PIN\_AG27 -to HEX0[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX0[3]

set\_location\_assignment PIN\_AF28 -to HEX0[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX0[4]

set\_location\_assignment PIN\_AG28 -to HEX0[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX0[5]

set\_location\_assignment PIN\_AH28 -to HEX0[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX0[6]

set\_location\_assignment PIN\_AJ29 -to HEX1[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX1[0]

set\_location\_assignment PIN\_AH29 -to HEX1[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX1[1]

set\_location\_assignment PIN\_AH30 -to HEX1[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX1[2]

set\_location\_assignment PIN\_AG30 -to HEX1[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX1[3]

set\_location\_assignment PIN\_AF29 -to HEX1[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX1[4]

set\_location\_assignment PIN\_AF30 -to HEX1[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX1[5]

set\_location\_assignment PIN\_AD27 -to HEX1[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX1[6]

set\_location\_assignment PIN\_AB23 -to HEX2[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX2[0]

set\_location\_assignment PIN\_AE29 -to HEX2[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX2[1]

set\_location\_assignment PIN\_AD29 -to HEX2[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX2[2]

set\_location\_assignment PIN\_AC28 -to HEX2[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX2[3]

set\_location\_assignment PIN\_AD30 -to HEX2[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX2[4]

set\_location\_assignment PIN\_AC29 -to HEX2[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX2[5]

set\_location\_assignment PIN\_AC30 -to HEX2[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX2[6]

set\_location\_assignment PIN\_AD26 -to HEX3[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX3[0]

set\_location\_assignment PIN\_AC27 -to HEX3[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX3[1]

set\_location\_assignment PIN\_AD25 -to HEX3[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX3[2]

set\_location\_assignment PIN\_AC25 -to HEX3[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX3[3]

set\_location\_assignment PIN\_AB28 -to HEX3[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX3[4]

set\_location\_assignment PIN\_AB25 -to HEX3[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX3[5]

set\_location\_assignment PIN\_AB22 -to HEX3[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX3[6]

set\_location\_assignment PIN\_AA24 -to HEX4[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX4[0]

set\_location\_assignment PIN\_Y23 -to HEX4[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX4[1]

set\_location\_assignment PIN\_Y24 -to HEX4[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX4[2]

set\_location\_assignment PIN\_W22 -to HEX4[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX4[3]

set\_location\_assignment PIN\_W24 -to HEX4[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX4[4]

set\_location\_assignment PIN\_V23 -to HEX4[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX4[5]

set\_location\_assignment PIN\_W25 -to HEX4[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX4[6]

set\_location\_assignment PIN\_V25 -to HEX5[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX5[0]

set\_location\_assignment PIN\_AA28 -to HEX5[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX5[1]

set\_location\_assignment PIN\_Y27 -to HEX5[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX5[2]

set\_location\_assignment PIN\_AB27 -to HEX5[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX5[3]

set\_location\_assignment PIN\_AB26 -to HEX5[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX5[4]

set\_location\_assignment PIN\_AA26 -to HEX5[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX5[5]

set\_location\_assignment PIN\_AA25 -to HEX5[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HEX5[6]

#============================================================

# IR

#============================================================

set\_location\_assignment PIN\_AA30 -to IRDA\_RXD

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to IRDA\_RXD

set\_location\_assignment PIN\_AB30 -to IRDA\_TXD

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to IRDA\_TXD

#============================================================

# KEY

#============================================================

set\_location\_assignment PIN\_AA14 -to KEY[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to KEY[0]

set\_location\_assignment PIN\_AA15 -to KEY[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to KEY[1]

set\_location\_assignment PIN\_W15 -to KEY[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to KEY[2]

set\_location\_assignment PIN\_Y16 -to KEY[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to KEY[3]

#============================================================

# LED

#============================================================

set\_location\_assignment PIN\_V16 -to LEDR[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to LEDR[0]

set\_location\_assignment PIN\_W16 -to LEDR[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to LEDR[1]

set\_location\_assignment PIN\_V17 -to LEDR[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to LEDR[2]

set\_location\_assignment PIN\_V18 -to LEDR[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to LEDR[3]

set\_location\_assignment PIN\_W17 -to LEDR[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to LEDR[4]

set\_location\_assignment PIN\_W19 -to LEDR[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to LEDR[5]

set\_location\_assignment PIN\_Y19 -to LEDR[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to LEDR[6]

set\_location\_assignment PIN\_W20 -to LEDR[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to LEDR[7]

set\_location\_assignment PIN\_W21 -to LEDR[8]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to LEDR[8]

set\_location\_assignment PIN\_Y21 -to LEDR[9]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to LEDR[9]

#============================================================

# PS2

#============================================================

set\_location\_assignment PIN\_AD7 -to PS2\_CLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to PS2\_CLK

set\_location\_assignment PIN\_AD9 -to PS2\_CLK2

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to PS2\_CLK2

set\_location\_assignment PIN\_AE7 -to PS2\_DAT

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to PS2\_DAT

set\_location\_assignment PIN\_AE9 -to PS2\_DAT2

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to PS2\_DAT2

#============================================================

# SW

#============================================================

set\_location\_assignment PIN\_AB12 -to SW[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to SW[0]

set\_location\_assignment PIN\_AC12 -to SW[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to SW[1]

set\_location\_assignment PIN\_AF9 -to SW[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to SW[2]

set\_location\_assignment PIN\_AF10 -to SW[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to SW[3]

set\_location\_assignment PIN\_AD11 -to SW[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to SW[4]

set\_location\_assignment PIN\_AD12 -to SW[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to SW[5]

set\_location\_assignment PIN\_AE11 -to SW[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to SW[6]

set\_location\_assignment PIN\_AC9 -to SW[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to SW[7]

set\_location\_assignment PIN\_AD10 -to SW[8]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to SW[8]

set\_location\_assignment PIN\_AE12 -to SW[9]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to SW[9]

#============================================================

# Video-In

#============================================================

set\_location\_assignment PIN\_H15 -to TD\_CLK27

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_CLK27

set\_location\_assignment PIN\_D2 -to TD\_DATA[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_DATA[0]

set\_location\_assignment PIN\_B1 -to TD\_DATA[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_DATA[1]

set\_location\_assignment PIN\_E2 -to TD\_DATA[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_DATA[2]

set\_location\_assignment PIN\_B2 -to TD\_DATA[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_DATA[3]

set\_location\_assignment PIN\_D1 -to TD\_DATA[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_DATA[4]

set\_location\_assignment PIN\_E1 -to TD\_DATA[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_DATA[5]

set\_location\_assignment PIN\_C2 -to TD\_DATA[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_DATA[6]

set\_location\_assignment PIN\_B3 -to TD\_DATA[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_DATA[7]

set\_location\_assignment PIN\_A5 -to TD\_HS

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_HS

set\_location\_assignment PIN\_F6 -to TD\_RESET\_N

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_RESET\_N

set\_location\_assignment PIN\_A3 -to TD\_VS

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to TD\_VS

#============================================================

# VGA

#============================================================

set\_location\_assignment PIN\_B13 -to VGA\_B[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_B[0]

set\_location\_assignment PIN\_G13 -to VGA\_B[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_B[1]

set\_location\_assignment PIN\_H13 -to VGA\_B[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_B[2]

set\_location\_assignment PIN\_F14 -to VGA\_B[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_B[3]

set\_location\_assignment PIN\_H14 -to VGA\_B[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_B[4]

set\_location\_assignment PIN\_F15 -to VGA\_B[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_B[5]

set\_location\_assignment PIN\_G15 -to VGA\_B[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_B[6]

set\_location\_assignment PIN\_J14 -to VGA\_B[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_B[7]

set\_location\_assignment PIN\_F10 -to VGA\_BLANK\_N

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_BLANK\_N

set\_location\_assignment PIN\_A11 -to VGA\_CLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_CLK

set\_location\_assignment PIN\_J9 -to VGA\_G[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_G[0]

set\_location\_assignment PIN\_J10 -to VGA\_G[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_G[1]

set\_location\_assignment PIN\_H12 -to VGA\_G[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_G[2]

set\_location\_assignment PIN\_G10 -to VGA\_G[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_G[3]

set\_location\_assignment PIN\_G11 -to VGA\_G[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_G[4]

set\_location\_assignment PIN\_G12 -to VGA\_G[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_G[5]

set\_location\_assignment PIN\_F11 -to VGA\_G[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_G[6]

set\_location\_assignment PIN\_E11 -to VGA\_G[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_G[7]

set\_location\_assignment PIN\_B11 -to VGA\_HS

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_HS

set\_location\_assignment PIN\_A13 -to VGA\_R[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_R[0]

set\_location\_assignment PIN\_C13 -to VGA\_R[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_R[1]

set\_location\_assignment PIN\_E13 -to VGA\_R[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_R[2]

set\_location\_assignment PIN\_B12 -to VGA\_R[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_R[3]

set\_location\_assignment PIN\_C12 -to VGA\_R[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_R[4]

set\_location\_assignment PIN\_D12 -to VGA\_R[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_R[5]

set\_location\_assignment PIN\_E12 -to VGA\_R[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_R[6]

set\_location\_assignment PIN\_F13 -to VGA\_R[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_R[7]

set\_location\_assignment PIN\_C10 -to VGA\_SYNC\_N

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_SYNC\_N

set\_location\_assignment PIN\_D11 -to VGA\_VS

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to VGA\_VS

#============================================================

# HPS

#============================================================

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_GTX\_CLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_INT\_N

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_MDC

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_MDIO

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_RX\_CLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_RX\_DATA[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_RX\_DATA[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_RX\_DATA[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_RX\_DATA[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_RX\_DV

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_TX\_DATA[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_TX\_DATA[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_TX\_DATA[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_TX\_DATA[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_ENET\_TX\_EN

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_FLASH\_DATA[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_FLASH\_DATA[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_FLASH\_DATA[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_FLASH\_DATA[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_FLASH\_DCLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_FLASH\_NCSO

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_GPIO[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_GPIO[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_GSENSOR\_INT

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_I2C1\_SCLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_I2C1\_SDAT

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_I2C2\_SCLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_I2C2\_SDAT

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_I2C\_CONTROL

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_KEY

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_LED

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_SD\_CLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_SD\_CMD

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_SD\_DATA[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_SD\_DATA[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_SD\_DATA[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_SD\_DATA[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_SPIM\_CLK

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_SPIM\_MISO

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_SPIM\_MOSI

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_SPIM\_SS

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_UART\_RX

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_UART\_TX

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_CLKOUT

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_DATA[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_DATA[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_DATA[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_DATA[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_DATA[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_DATA[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_DATA[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_DATA[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_DIR

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_NXT

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_USB\_STP

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to HPS\_CONV\_USB\_N

#============================================================

# GPIO\_0, GPIO\_0 connect to GPIO Default

#============================================================

set\_location\_assignment PIN\_AC18 -to GPIO\_0[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[0]

set\_location\_assignment PIN\_Y17 -to GPIO\_0[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[1]

set\_location\_assignment PIN\_AD17 -to GPIO\_0[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[2]

set\_location\_assignment PIN\_Y18 -to GPIO\_0[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[3]

set\_location\_assignment PIN\_AK16 -to GPIO\_0[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[4]

set\_location\_assignment PIN\_AK18 -to GPIO\_0[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[5]

set\_location\_assignment PIN\_AK19 -to GPIO\_0[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[6]

set\_location\_assignment PIN\_AJ19 -to GPIO\_0[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[7]

set\_location\_assignment PIN\_AJ17 -to GPIO\_0[8]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[8]

set\_location\_assignment PIN\_AJ16 -to GPIO\_0[9]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[9]

set\_location\_assignment PIN\_AH18 -to GPIO\_0[10]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[10]

set\_location\_assignment PIN\_AH17 -to GPIO\_0[11]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[11]

set\_location\_assignment PIN\_AG16 -to GPIO\_0[12]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[12]

set\_location\_assignment PIN\_AE16 -to GPIO\_0[13]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[13]

set\_location\_assignment PIN\_AF16 -to GPIO\_0[14]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[14]

set\_location\_assignment PIN\_AG17 -to GPIO\_0[15]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[15]

set\_location\_assignment PIN\_AA18 -to GPIO\_0[16]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[16]

set\_location\_assignment PIN\_AA19 -to GPIO\_0[17]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[17]

set\_location\_assignment PIN\_AE17 -to GPIO\_0[18]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[18]

set\_location\_assignment PIN\_AC20 -to GPIO\_0[19]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[19]

set\_location\_assignment PIN\_AH19 -to GPIO\_0[20]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[20]

set\_location\_assignment PIN\_AJ20 -to GPIO\_0[21]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[21]

set\_location\_assignment PIN\_AH20 -to GPIO\_0[22]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[22]

set\_location\_assignment PIN\_AK21 -to GPIO\_0[23]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[23]

set\_location\_assignment PIN\_AD19 -to GPIO\_0[24]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[24]

set\_location\_assignment PIN\_AD20 -to GPIO\_0[25]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[25]

set\_location\_assignment PIN\_AE18 -to GPIO\_0[26]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[26]

set\_location\_assignment PIN\_AE19 -to GPIO\_0[27]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[27]

set\_location\_assignment PIN\_AF20 -to GPIO\_0[28]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[28]

set\_location\_assignment PIN\_AF21 -to GPIO\_0[29]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[29]

set\_location\_assignment PIN\_AF19 -to GPIO\_0[30]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[30]

set\_location\_assignment PIN\_AG21 -to GPIO\_0[31]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[31]

set\_location\_assignment PIN\_AF18 -to GPIO\_0[32]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[32]

set\_location\_assignment PIN\_AG20 -to GPIO\_0[33]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[33]

set\_location\_assignment PIN\_AG18 -to GPIO\_0[34]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[34]

set\_location\_assignment PIN\_AJ21 -to GPIO\_0[35]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_0[35]

#============================================================

# GPIO\_1, GPIO\_1 connect to GPIO Default

#============================================================

set\_location\_assignment PIN\_AB17 -to GPIO\_1[0]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[0]

set\_location\_assignment PIN\_AA21 -to GPIO\_1[1]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[1]

set\_location\_assignment PIN\_AB21 -to GPIO\_1[2]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[2]

set\_location\_assignment PIN\_AC23 -to GPIO\_1[3]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[3]

set\_location\_assignment PIN\_AD24 -to GPIO\_1[4]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[4]

set\_location\_assignment PIN\_AE23 -to GPIO\_1[5]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[5]

set\_location\_assignment PIN\_AE24 -to GPIO\_1[6]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[6]

set\_location\_assignment PIN\_AF25 -to GPIO\_1[7]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[7]

set\_location\_assignment PIN\_AF26 -to GPIO\_1[8]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[8]

set\_location\_assignment PIN\_AG25 -to GPIO\_1[9]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[9]

set\_location\_assignment PIN\_AG26 -to GPIO\_1[10]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[10]

set\_location\_assignment PIN\_AH24 -to GPIO\_1[11]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[11]

set\_location\_assignment PIN\_AH27 -to GPIO\_1[12]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[12]

set\_location\_assignment PIN\_AJ27 -to GPIO\_1[13]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[13]

set\_location\_assignment PIN\_AK29 -to GPIO\_1[14]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[14]

set\_location\_assignment PIN\_AK28 -to GPIO\_1[15]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[15]

set\_location\_assignment PIN\_AK27 -to GPIO\_1[16]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[16]

set\_location\_assignment PIN\_AJ26 -to GPIO\_1[17]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[17]

set\_location\_assignment PIN\_AK26 -to GPIO\_1[18]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[18]

set\_location\_assignment PIN\_AH25 -to GPIO\_1[19]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[19]

set\_location\_assignment PIN\_AJ25 -to GPIO\_1[20]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[20]

set\_location\_assignment PIN\_AJ24 -to GPIO\_1[21]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[21]

set\_location\_assignment PIN\_AK24 -to GPIO\_1[22]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[22]

set\_location\_assignment PIN\_AG23 -to GPIO\_1[23]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[23]

set\_location\_assignment PIN\_AK23 -to GPIO\_1[24]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[24]

set\_location\_assignment PIN\_AH23 -to GPIO\_1[25]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[25]

set\_location\_assignment PIN\_AK22 -to GPIO\_1[26]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[26]

set\_location\_assignment PIN\_AJ22 -to GPIO\_1[27]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[27]

set\_location\_assignment PIN\_AH22 -to GPIO\_1[28]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[28]

set\_location\_assignment PIN\_AG22 -to GPIO\_1[29]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[29]

set\_location\_assignment PIN\_AF24 -to GPIO\_1[30]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[30]

set\_location\_assignment PIN\_AF23 -to GPIO\_1[31]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[31]

set\_location\_assignment PIN\_AE22 -to GPIO\_1[32]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[32]

set\_location\_assignment PIN\_AD21 -to GPIO\_1[33]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[33]

set\_location\_assignment PIN\_AA20 -to GPIO\_1[34]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[34]

set\_location\_assignment PIN\_AC22 -to GPIO\_1[35]

set\_instance\_assignment -name IO\_STANDARD "3.3-V LVTTL" -to GPIO\_1[35]

Figure 10. DE1-SoC Pin Assignment TCL Script

### FPGA & HPS

This is where the Cyclone V starts getting complicated to use as many steps are needed before being able to use the HPS. We will first begin by looking at how the HPS boots.

Bare-metal vs Linux

Requires an explanation of “booting”

## Software

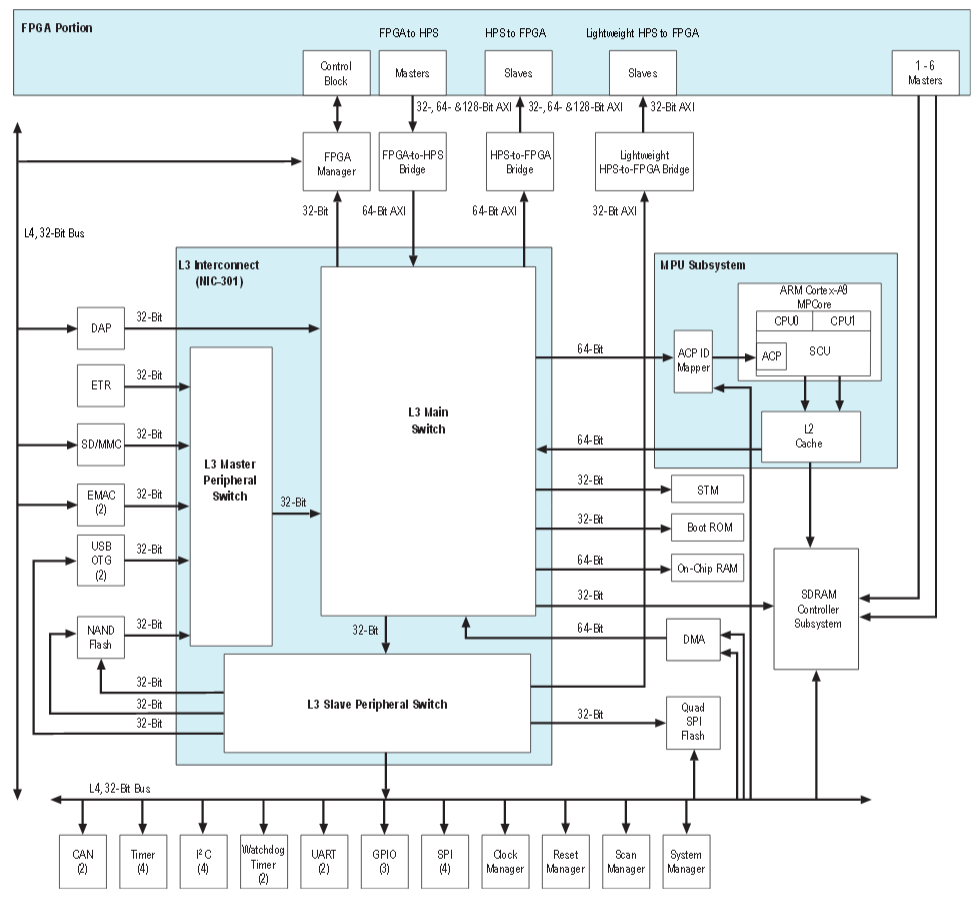
# todo

explain MSEL when reprogramming the FPGA from the HPS.

# SoC part test

## HPS Architecture

To be able to program the ARM9’s processors it is almost necessary to have the global view of the HPS architecture.



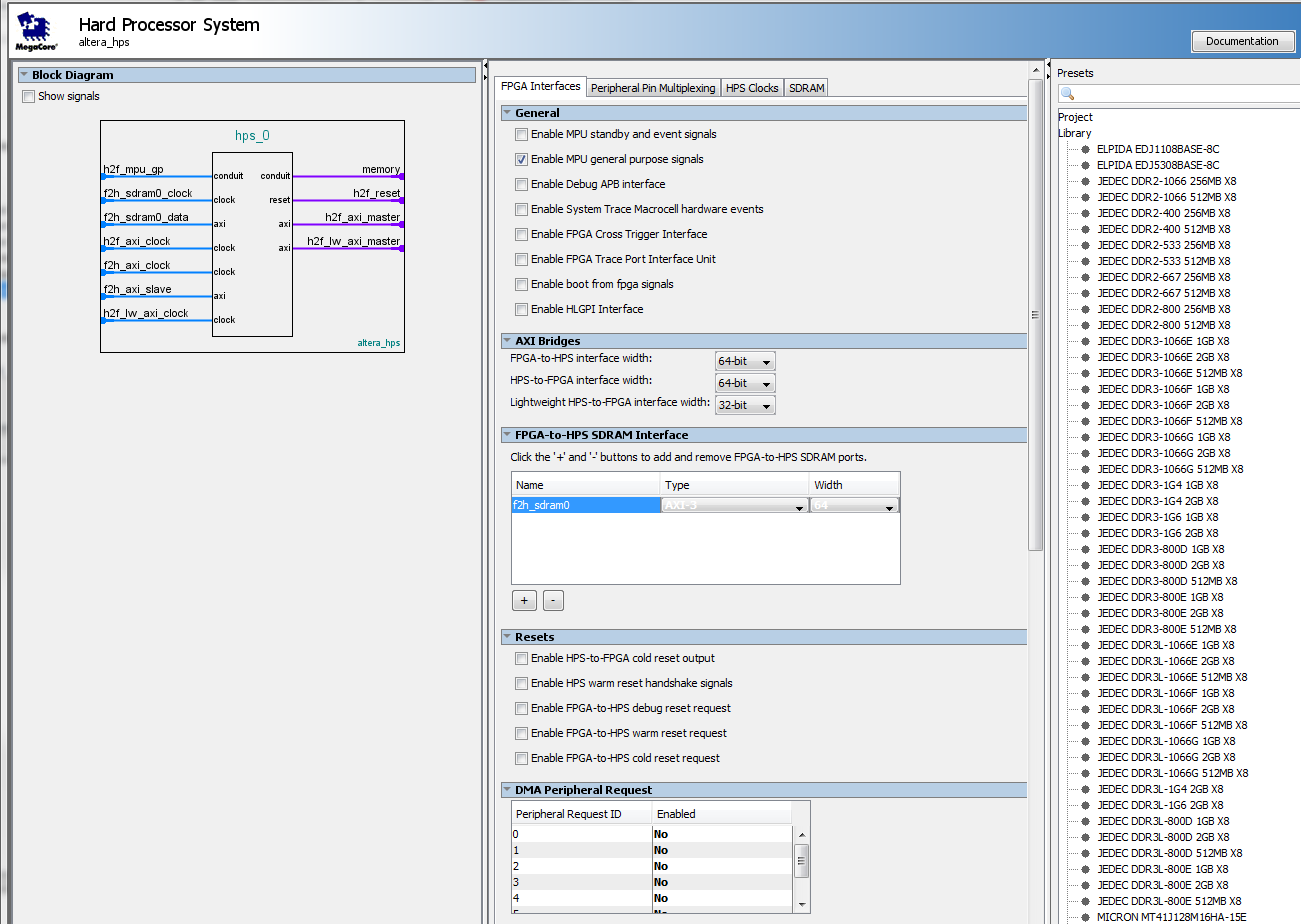
## Hardware development

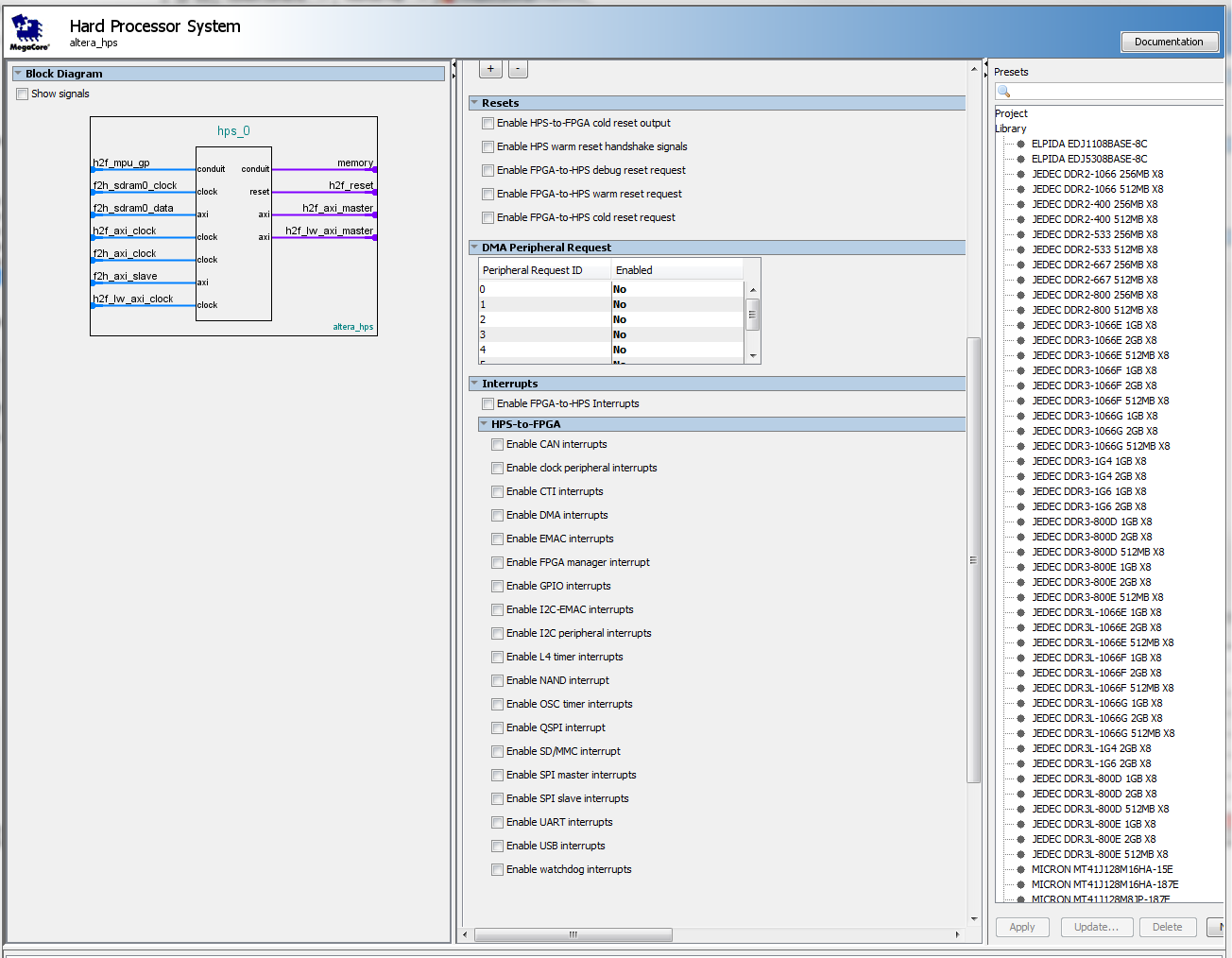
### Qsys integration

Starting with **QuartusII** and after creating a project, select ***Tools🡪 Qsys***

In **Qsys**, open ***Library 🡪 Embedded Processors 🡪 Hard Processor System*** the window with description of the parameters for the HPS is open.

The ***FPGA Interface*** tab allows the access from to the FPGA part with the HPS part.





With the ***PeripheralPin Multiplexing***, some I/O interface can be used by the HPS part or the FPGA part. The selection is done here.

## Software development

### ARM DS-5 tools

They are some differences between the versions of DS-5.

The one installed for the test is:

ARM DS-5 (DS-5 Altera Edition (Evaluation))

Version: 5.18.0

Build number: 5180018

### Hello World on ARM HPS part

Copy the directory from Altera examples:

C:\altera\13.1\embedded\examples\software

And un-gz the file: Altera-SoCFPGA-HelloWorld-Baremetal-ARMCC.tar.gz

Then un-tar it.

The directory **Altera-SoCFPGA-HelloWorld-Baremetal-ARMCC** can then be copied in the Eclipse WorkSpace and Imported as a new project. The files inside are:

* .cproject used by Eclipse
* . project used by Eclipse
* \*\*\*\*.launch ??
* Makefile for the Compiler/Assembler/Linker  
   An important info is the flag for the cpu: --cpu=Cortex-A9.no\_neon.no\_vfp
* scatter.scat Info for the compiler for the Code, Data, Stack and Heap addresses  
   in this case in the internal SRAM

#### Scatter.scat

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; Copyright (c) 2013 Altera All Rights Reserved.

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; Scatter-file for OnChip RAM based example

; This scatter-file places application code, data, stack and heap at suitable addresses in the memory map.

; Altera SoC-FPGA has **64kB of internal OnChip RAM**

**OCRAM 0xFFFF0000 0x10000**

{

APP\_CODE +0

{

\* (+RO, +RW, +ZI)

}

ARM\_LIB\_STACKHEAP 0xFFFF8000 EMPTY 0x8000 ; Application heap and stack

{ }

}

#### Makefile

Makefile for the ARM compiler

# Copyright (C) ARM Limited, 2011. All rights reserved.

#

# This example is intended to be built with the ARM Compiler armcc

TARGET=Altera-SoCFPGA-HelloWorld-Baremetal-ARMCC.axf

CC=armcc

AS=armasm

LD=armlink

AR=armar

# Select build rules based on Windows or Unix

ifdef WINDIR

DONE=@if exist $(1) echo Build completed.

RM=if exist $(1) del /q $(1)

SHELL=$(WINDIR)\system32\cmd.exe

else

ifdef windir

DONE=@if exist $(1) echo Build completed.

RM=if exist $(1) del /q $(1)

SHELL=$(windir)\system32\cmd.exe

else

DONE=@if [ -f $(1) ]; then echo Build completed.; fi

RM=rm -f $(1)

endif

endif

all: $(TARGET)

$(call DONE,$(TARGET))

rebuild: clean all

clean:

$(call RM,\*.o)

$(call RM,$(TARGET))

hello.o: hello.c

$(CC) -c -g --cpu=Cortex-A9.no\_neon.no\_vfp -O0 hello.c

$(TARGET): hello.o scatter.scat

$(LD) hello.o -o $(TARGET) --cpu=Cortex-A9.no\_neon.no\_vfp --scatter=scatter.scat

### GPIO access

The references for gpio are:

* <http://www.altera.com/literature/hb/cyclone-v/cv_54022.pdf>
* <http://www.altera.com/literature/hb/cyclone-v/hps.html>
* Supports up to 71 I/O pins and 14 input-only pins depend on device variant

On de1-soc:

* Only 1 Button for HPS GPIO 1
* Only 1 LED for HPS GPIO 1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Pin Name** | **HPS GPIO** | **Register [bit]** | **Function** | **Address** | **Dir** |
| HPS\_KEY | GPIO54 | GPIO1[25] | I/O | 0xFF20 9000 | In |
| HPS\_LED | GPIO53 | GPIO1[24] | I/O | 0xFF20 9000 | Out |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

HPS peripherals are mapped to HPS base address space 0xFC00 0000 with 64KB size.

Registers of GPIO0 controller are mapped to the base address 0xFF20 8000 - 0xFF20 8FFF (4KB size)

Registers of GPIO1 controller are mapped to the base address 0xFF20 9000 - 0xFF20 9FFF (4KB size)

Registers of GPIO2 controller are mapped to the base address 0xFF20 A000 - 0xFF20 8FFF (4KB size)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | http://www.altera.com/literature/hb/cyclone-v/cv\_5v4.pdf |  |  |
| GPIO0 | 0xFF20 8000 - 0xFF20 8FFF | 0xFF70 8000 |  |  |
| GPIO1 | 0xFF20 9000 - 0xFF20 9FFF | 0xFF70 9000 |  |  |
| GPIO2 | 0xFF20 A000 - 0xFF20 8FFF | 0xFF70 A000 |  |  |
| LWFPGASLAVES |  | 0xFF20 0000 |  |  |
|  |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |
| gpio0 | 0xFF70 8000 | HPS\_GPIO0\_ADDRESS | HPS\_GPIO0\_OFFSET |  |  |
| gpio\_swporta\_dr | 0 | HPS\_GPIO0\_GPIO\_SWPORTA\_DR\_ADDRESS | GPIO\_GPIO\_SWPORTA\_DR\_OFFSET |  |  |
| gpio\_swporta\_ddr | 0x04 | HPS\_GPIO0\_GPIO\_SWPORTA\_DDR\_ADDRESS | GPIO\_GPIO\_SWPORTA\_DDR\_OFFSET |  |  |
| gpio\_inten | 0x30 | HPS\_GPIO0\_GPIO\_INTEN\_ADDRESS | GPIO\_GPIO\_INTEN\_OFFSET |  |  |
| gpio\_intmask | 0x34 | HPS\_GPIO0\_GPIO\_INTMASK\_ADDRESS | GPIO\_GPIO\_INTMASK\_OFFSET |  |  |
| gpio\_inttype\_level | 0x38 | HPS\_GPIO0\_GPIO\_INTTYPE\_LEVEL\_ADDRESS | GPIO\_GPIO\_INTTYPE\_LEVEL\_OFFSET |  |  |
| gpio\_int\_polarity | 0x3c | HPS\_GPIO0\_GPIO\_INT\_POLARITY\_ADDRESS | GPIO\_GPIO\_INT\_POLARITY\_OFFSET |  |  |
| gpio\_intstatus | 0x40 | HPS\_GPIO0\_GPIO\_INTSTATUS\_ADDRESS | GPIO\_GPIO\_INTSTATUS\_OFFSET |  |  |
| gpio\_raw\_intstatus | 0x44 | HPS\_GPIO0\_GPIO\_RAW\_INTSTATUS\_ADDRESS | GPIO\_GPIO\_RAW\_INTSTATUS\_OFFSET |  |  |
| gpio\_debounce | 0x48 | HPS\_GPIO0\_GPIO\_DEBOUNCE\_ADDRESS | GPIO\_GPIO\_DEBOUNCE\_OFFSET |  |  |
| gpio\_porta\_eoi | 0x4c | HPS\_GPIO0\_GPIO\_PORTA\_EOI\_ADDRESS | GPIO\_GPIO\_PORTA\_EOI\_OFFSET |  |  |
| gpio\_ext\_porta | 0x50 | HPS\_GPIO0\_GPIO\_EXT\_PORTA\_ADDRESS | GPIO\_GPIO\_EXT\_PORTA\_OFFSET |  |  |
| gpio\_ls\_sync | 0x60 | HPS\_GPIO0\_GPIO\_LS\_SYNC\_ADDRESS | GPIO\_GPIO\_LS\_SYNC\_OFFSET |  |  |
| gpio\_id\_code | 0x64 | HPS\_GPIO0\_GPIO\_ID\_CODE\_ADDRESS | GPIO\_GPIO\_ID\_CODE\_OFFSET |  |  |
| gpio\_ver\_id\_code | 0x6c | HPS\_GPIO0\_GPIO\_VER\_ID\_CODE\_ADDRESS | GPIO\_GPIO\_VER\_ID\_CODE\_OFFSET |  |  |
| gpio\_config\_reg2 | 0x70 | HPS\_GPIO0\_GPIO\_CONFIG\_REG2\_ADDRESS | GPIO\_GPIO\_CONFIG\_REG2\_OFFSET |  |  |
| gpio\_config\_reg1 | 0x74 | HPS\_GPIO0\_GPIO\_CONFIG\_REG1\_ADDRESS | GPIO\_GPIO\_CONFIG\_REG1\_OFFSET |  |  |
|  |  |  |  |  |  |

#### Library installation

C:\altera\13.1\embedded\ip\altera\hps\altera\_hps\hwlib

HERE

#### Reference files

|  |  |  |
| --- | --- | --- |
| hps.h |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

##### Titre5

###### Titre6

Titre7

Titre8

Titre9

References

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  <http://www.altera.com/literature/lit-cyclone-v.jsp?ln=devices_fpga&l3=Low-Cost%20FPGAs-Cyclone%20V%20%28E,%20GX,%20GT,%20SE,%20SX,%20ST%29&l4=Documentation>
* Cyclone V Device Handbook Volume 3: Hard Processor System Technical Reference Manual  
  <http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf>
* Cyclone V Hard Processor System User Guide   
  <http://www.altera.com/literature/hb/cyclone-v/cv_5v4_08.pdf>
* Cyclone V, Device Datasheet   
  <http://www.altera.com/literature/hb/cyclone-v/cv_51002.pdf>
* Cylone V HPS addresses   
  <http://www.altera.com/literature/hb/cyclone-v/hps.html>
* Cyclone V Device Handbook Volume 1: Device Interfaces and Integration  
  <http://www.altera.com/literature/hb/cyclone-v/cyclone5_handbook.pdf>
* Cyclone V, Device Overview  
  <http://www.altera.com/literature/hb/cyclone-v/cv_51001.pdf>
* SoCAL documentation (html), The Altera SoC Abstraction Layer (SoCAL) API Reference Manual  
  <file:///C:/altera/13.1/embedded/ip/altera/hps/altera_hps/doc/socal/html/index.html>
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  <http://www.youtube.com/watch?v=CJ0EHJ9oQ7Y>
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  <http://www.youtube.com/watch?v=RVM-ESUMOMU> (Part 1 of 5)  
  <http://www.youtube.com/watch?v=Ssxf8ggmQk4> (Part 2 of 5)  
  <http://www.youtube.com/watch?v=cWIaqt2RU84> (Part 3 of 5)  
  <http://www.youtube.com/watch?v=gUE669XKhUY> (Part 4 of 5)  
  <http://www.youtube.com/watch?v=NxZznvf5EKc> (Part 5 of 5)
* DS-5 Altera Edition: Bare-metal Debug and Trace  
  <http://www.youtube.com/watch?v=u_xKybPhcHI>
* OpenCL on FPGAs Accelerating Performance and Design Productivity — Altera   
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