SoC-FPGA Design

Manual

Real Time Embedded Systems Course

LAP – IC – EPFL

Version 0.4 (Preliminary)

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# Introduction

The development of embedded systems based on chips containing one or more microprocessors and hardcore peripherals, as well as an FPGA part is becoming more and more important. This technology gives the designer a lot of freedom and powerful abilities. Classical design flows with microcontrollers are emphasized with the full power of FPGAs.

Mixed designs are becoming a reality with. One can now design specific accelerators to greatly improve algorithms, or create specific programmable interfaces with the external world.

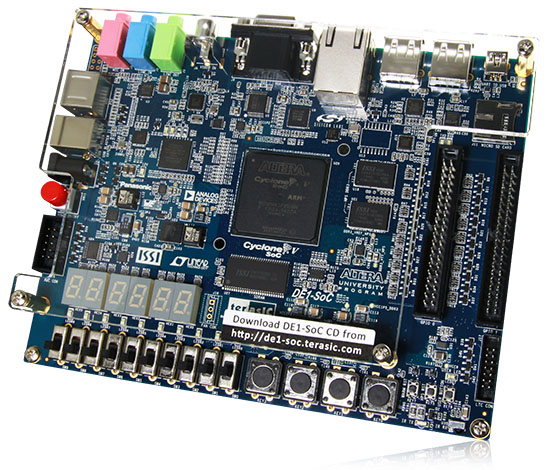
Two main HDL (**H**ardware **D**esign **L**anguage) languages are available for the design of the FPGA part: **VHDL** and Verilog. There also exist other tools that perform automatic translations from C to HDL. New emerging technologies like OpenCL allow compatibility between high-level software design, and low-level hardware implementations as:

* Compilation for single or multicore processors
* Compilation for GPUs (Graphical Processing Unit)
* Translation and compilation for FPGAs. The latest models use a PCIe interface or some other way of parameters passing between the main processor and the FPGA

*This guide assumes users know how to use QuartusII, NIOSII, Qsys and ModelSim-Altera.*

We will be using the Terasic DE1-SoC board: <http://de1-soc.terasic.com>

# Terasic DE1-SoC Board



Terasic DE1-SoC Board

The DE1-SoC board has many features that allow users to implement a wide range of designed circuits. We will discuss some noteworthy features in this guide.

## Specifications

FPGA Device

* Cyclone V SoC **5CSEMA5F31C6** Device
* Dual-core **ARM Cortex-A9** (HPS)
* **85K** Programmable Logic Elements
* 4’450 Kbits embedded memory
* 6 Fractional PLLs
* 2 Hard Memory Controllers

Configuration and Debug

* Quad Serial Configuration device – **EPCQ256** on FPGA
* On-Board **USB Blaster II** (Normal type B USB connector)

Memory Device

* **64MB** (32Mx16) SDRAM on FPGA
* **1GB** (2x256Mx16) DDR3 SDRAM on HPS
* **Micro SD** Card Socket on HPS

Communication

* Two Port USB 2.0 Host (ULPI interface with USB type A connector)
* USB to UART (micro USB type B connector)
* 10/100/1000 Ethernet
* PS/2 mouse/keyboard
* IR Emitter/Receiver

Connectors

* Two 40-pin Expansion Headers
* One 10-pin ADC Input Header
* One LTC connector (One Serial Peripheral Interface (SPI) Master, one I2C and one GPIO interface)

Display

* 24-bit VGA DAC

Audio

* 24-bit CODEC, line-in, line-out, and microphone-in jacks

Video Input

* TV Decoder (NTSC/PAL/SECAM) and TV-in connector

ADC

* Fast throughput rate: 1 MSPS
* Channel number: 8
* Resolution: 12 bits
* Analog input range : 0 ~ 2.5 V or 0 ~ 5V as selected via the RANGE bit in the control register

Switches, Buttons and Indicators

* 4 User Keys (FPGA x4)
* 10 User switches (FPGA x10)
* 11 User LEDs (FPGA x10; HPS x 1)
* 2 HPS Reset Buttons (HPS\_RST\_n and HPS\_WARM\_RST\_n)
* Six 7-segment displays

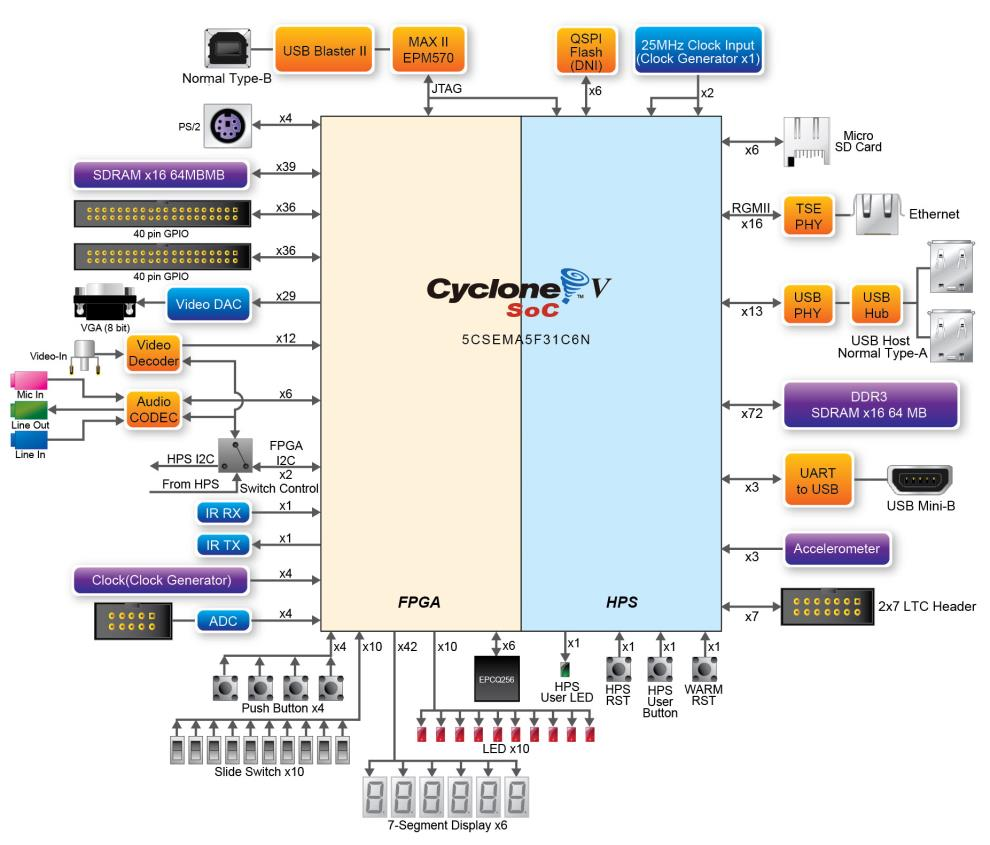
Sensors

* G-Sensor on HPS

Power

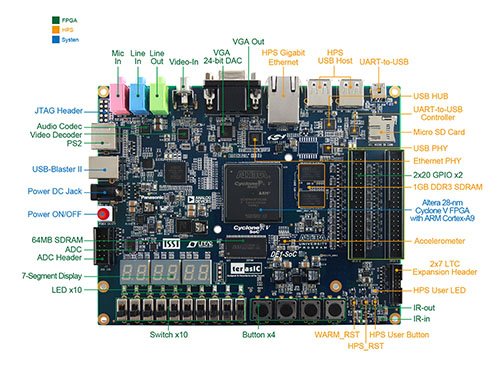
* 12V DC input

Block Diagram

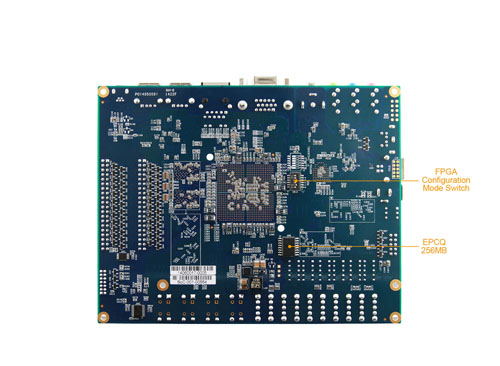


1. Block Diagram of the DE1-SoC Board

## Layout



1. Front



Back

* Green for peripherals directly connected to the FPGA
* Orange for peripherals directly connected to the HPS
* Blue for board control

Manuals and resources are available on the DE1-SoC [resources](http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=165&No=836&PartNo=4ParagrapheTexte) page.

# Cyclone V Overview

This section describes some features of the Cyclone V family of devices. All this information, along with the most complete documentation regarding this family can be found on the [Cyclone V Device Handbook](http://www.altera.com/literature/hb/cyclone-v/cyclone5_handbook.pdf), more specifically [Volume 3: Hard Processor System Technical Reference Manual](http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf).

## Introduction to the Cyclone V Hard Processor System

The Cyclone V device is a single-die system on a chip (SoC) that consists of two distinct parts – a hard processor system (HPS) portion and an FPGA portion.



Altera SoC FPGA Device Block Diagram

The HPS contains a microprocessor unit (MPU) subsystem with single or dual ARM Cortex-A9 MPCore processors, flash memory controllers, SDRAM L3 Interconnect, on-chip memories, support peripherals, interface peripherals, debug capabilities, and phase-locked loops (PLLs). The dual-processor HPS supports symmetric (SMP) and asymmetric (AMP) multiprocessing.

The DE1-SoC has a dual-processor HPS.

The FPGA portion of the device contains the FPGA fabric, a control block (CB), phase-locked loops (PLLs), and depending on the device variant, high-speed serial interface (HSSI) transceivers, hard PCI Express (PCIe) controllers, and hard memory controllers.

The DE1-SoC doesn’t contain any HSSI transceivers, or hard PCIe controllers.

The HPS and FPGA portions of the device are distinctly different. The HPS can boot from multiple sources, including the FPGA fabric and external flash. In contrast, the FPGA must be configured through either the HPS or an externally supported device.

The MPU subsystem can boot from flash devices connected to the HPS pins. Or, when the FPGA portion is configured by an external source, the MPU subsystem can boot from memory available on the FPGA portion of the device.

The HPS and FPGA portions of the device each have their own pins. Pins are not freely shared between the HPS and the FPGA fabric. The FPGA I/O pins are configured by an FPGA configuration image through the HPS or any external source supported by the device. The HPS I/O pins are configured by software executing in the HPS. Software executing on the HPS accesses control registers in the system manager to assign HPS I/O pins to the available HPS modules.

The software that configures the HPS I/O pins is called the Preloader.

The HPS and FPGA portions of the device have separate external power supplies and independently power on. You can power on the HPS without powering on the FPGA portion of the device. However, to power on the FPGA portion, the HPS must already be on or powered on at the same time as the FPGA portion. You can also turn off the FPGA portion of the device while leaving the HPS power on.

## Features of the HPS

The following list contains the main modules of the HPS:

* MPU subsystem featuring dual ARM Cortex-A9 MPCore processors
* General-purpose Direct Memory Access (DMA) controller
* Two Ethernet media access controllers (EMACs)
* Two USB 2.0 On-The-Go (OTG) controllers
* NAND flash controller
* Quad SPI flash controller
* Secure Digital (SD) / MultiMediaCard (MMC) controller
* Two serial peripheral interface (SPI) master controllers
* Two SPI slave controllers
* Four inter-integrated circuit (I2C) controllers
* 64 KB on-chip RAM
* 64 KB on-chip boot ROM
* Two UARTs
* Four timers
* Two watchdog timers
* Three general-purpose I/O (GPIO) interfaces
* Two controller area network (CAN) controllers
* ARM CoreSight debug components
* System manager
* Clock manager
* Reset manager
* Scan manager
* FPGA manager

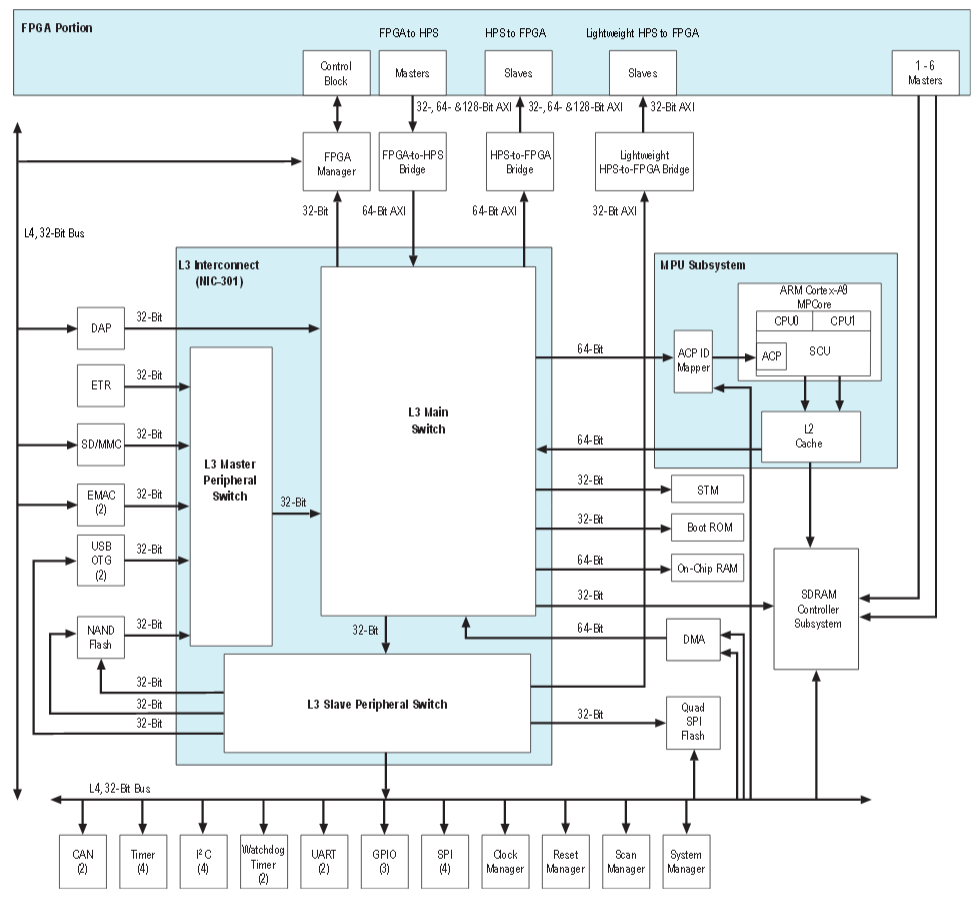
## HPS Block Diagram



# SoC part test

## HPS Architecture

To be able to program the ARM9’s processors it is almost necessary to have the global view of the HPS architecture.



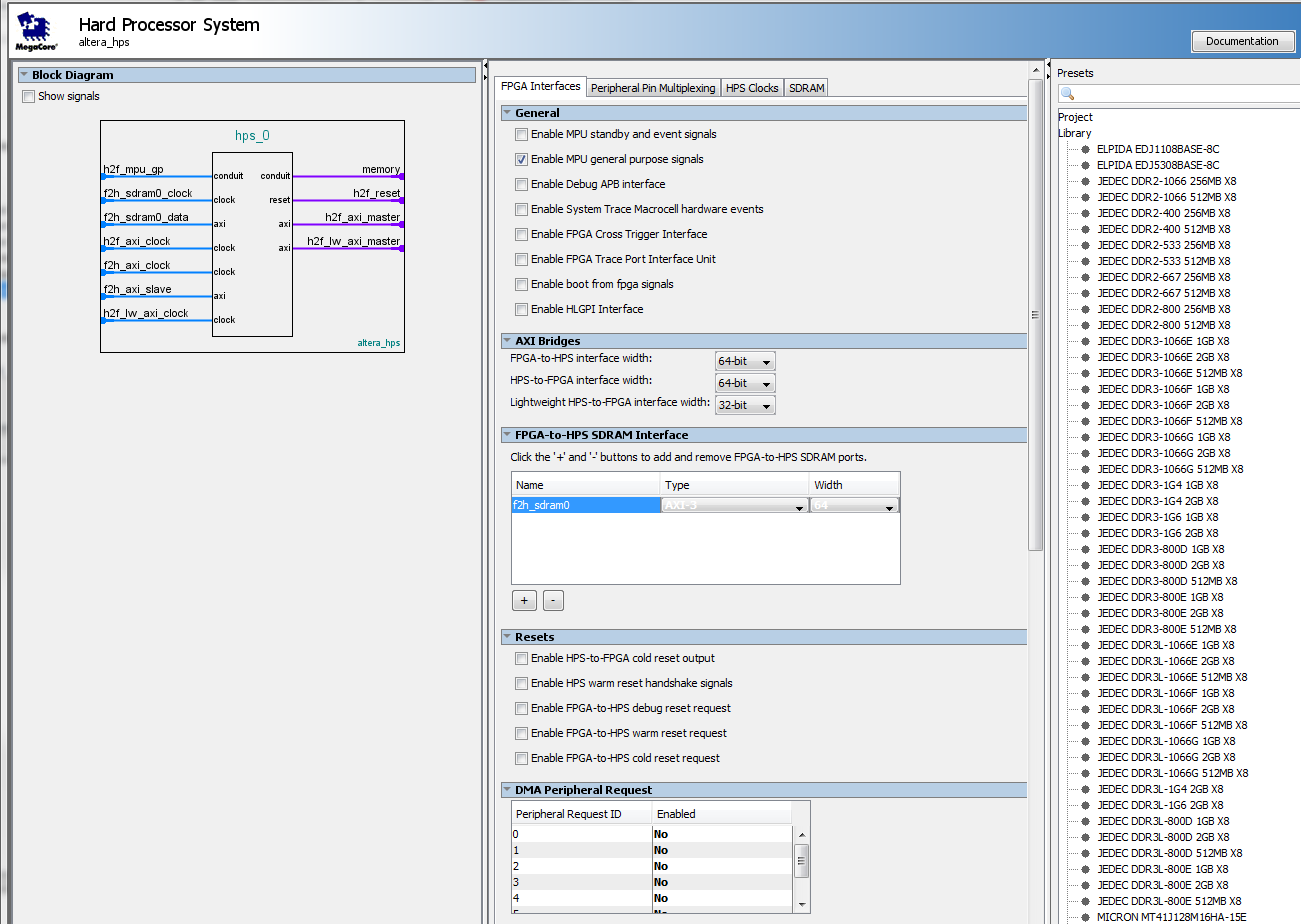
## Hardware development

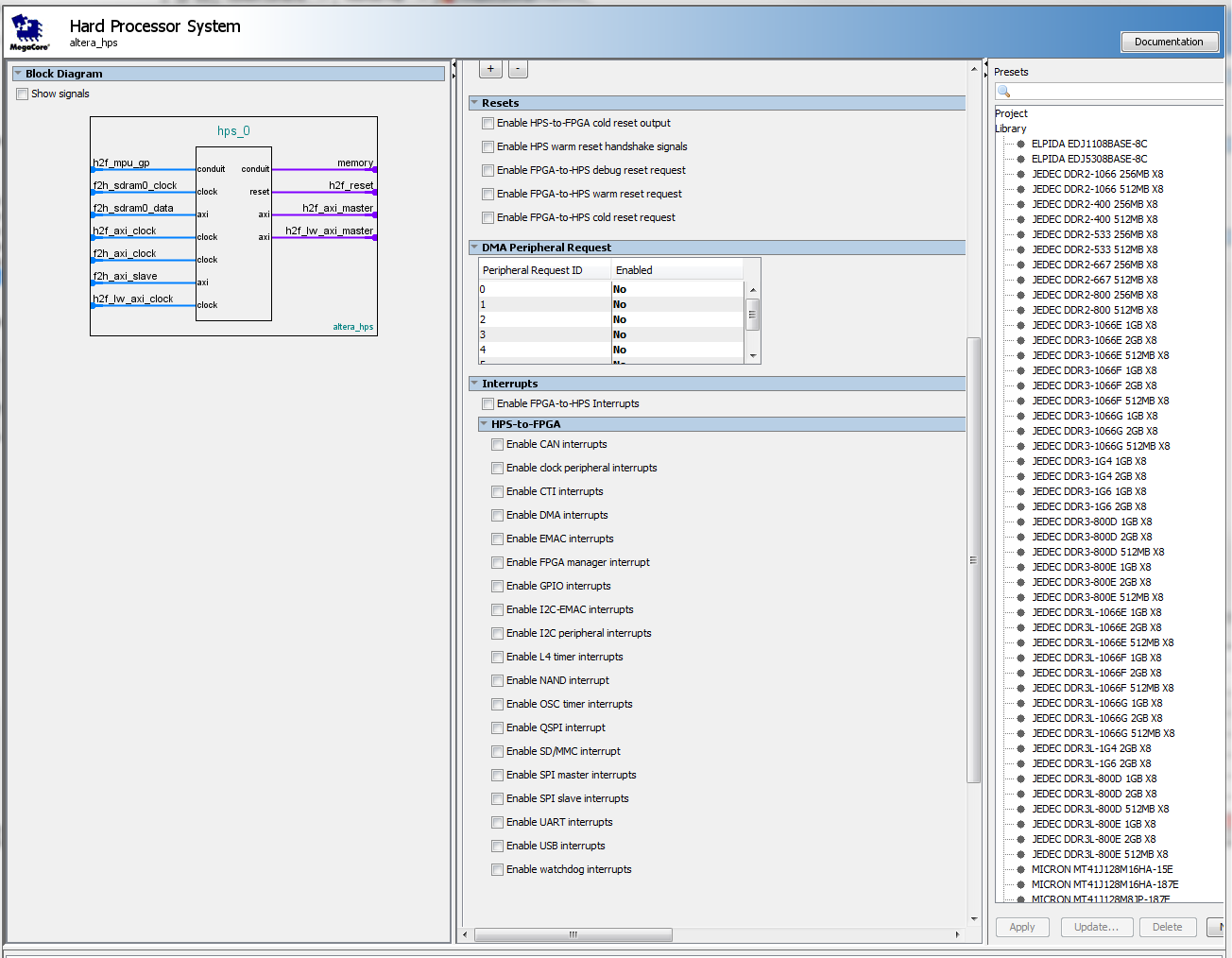
### Qsys integration

Starting with **QuartusII** and after creating a project, select ***Tools🡪 Qsys***

In **Qsys**, open ***Library 🡪 Embedded Processors 🡪 Hard Processor System*** the window with description of the parameters for the HPS is open.

The ***FPGA Interface*** tab allows the access from to the FPGA part with the HPS part.





With the ***PeripheralPin Multiplexing***, some I/O interface can be used by the HPS part or the FPGA part. The selection is done here.

## Software development

### ARM DS-5 tools

They are some differences between the versions of DS-5.

The one installed for the test is:

ARM DS-5 (DS-5 Altera Edition (Evaluation))

Version: 5.18.0

Build number: 5180018

### Hello World on ARM HPS part

Copy the directory from Altera examples:

C:\altera\13.1\embedded\examples\software

And un-gz the file: Altera-SoCFPGA-HelloWorld-Baremetal-ARMCC.tar.gz

Then un-tar it.

The directory **Altera-SoCFPGA-HelloWorld-Baremetal-ARMCC** can then be copied in the Eclipse WorkSpace and Imported as a new project. The files inside are:

* .cproject used by Eclipse
* . project used by Eclipse
* \*\*\*\*.launch ??
* Makefile for the Compiler/Assembler/Linker  
   An important info is the flag for the cpu: --cpu=Cortex-A9.no\_neon.no\_vfp
* scatter.scat Info for the compiler for the Code, Data, Stack and Heap addresses  
   in this case in the internal SRAM

#### Scatter.scat

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; Copyright (c) 2013 Altera All Rights Reserved.

;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; Scatter-file for OnChip RAM based example

; This scatter-file places application code, data, stack and heap at suitable addresses in the memory map.

; Altera SoC-FPGA has **64kB of internal OnChip RAM**

**OCRAM 0xFFFF0000 0x10000**

{

APP\_CODE +0

{

\* (+RO, +RW, +ZI)

}

ARM\_LIB\_STACKHEAP 0xFFFF8000 EMPTY 0x8000 ; Application heap and stack

{ }

}

#### Makefile

Makefile for the ARM compiler

# Copyright (C) ARM Limited, 2011. All rights reserved.

#

# This example is intended to be built with the ARM Compiler armcc

TARGET=Altera-SoCFPGA-HelloWorld-Baremetal-ARMCC.axf

CC=armcc

AS=armasm

LD=armlink

AR=armar

# Select build rules based on Windows or Unix

ifdef WINDIR

DONE=@if exist $(1) echo Build completed.

RM=if exist $(1) del /q $(1)

SHELL=$(WINDIR)\system32\cmd.exe

else

ifdef windir

DONE=@if exist $(1) echo Build completed.

RM=if exist $(1) del /q $(1)

SHELL=$(windir)\system32\cmd.exe

else

DONE=@if [ -f $(1) ]; then echo Build completed.; fi

RM=rm -f $(1)

endif

endif

all: $(TARGET)

$(call DONE,$(TARGET))

rebuild: clean all

clean:

$(call RM,\*.o)

$(call RM,$(TARGET))

hello.o: hello.c

$(CC) -c -g --cpu=Cortex-A9.no\_neon.no\_vfp -O0 hello.c

$(TARGET): hello.o scatter.scat

$(LD) hello.o -o $(TARGET) --cpu=Cortex-A9.no\_neon.no\_vfp --scatter=scatter.scat

### GPIO access

The references for gpio are:

* <http://www.altera.com/literature/hb/cyclone-v/cv_54022.pdf>
* <http://www.altera.com/literature/hb/cyclone-v/hps.html>
* Supports up to 71 I/O pins and 14 input-only pins depend on device variant

On de1-soc:

* Only 1 Button for HPS GPIO 1
* Only 1 LED for HPS GPIO 1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Pin Name** | **HPS GPIO** | **Register [bit]** | **Function** | **Address** | **Dir** |
| HPS\_KEY | GPIO54 | GPIO1[25] | I/O | 0xFF20 9000 | In |
| HPS\_LED | GPIO53 | GPIO1[24] | I/O | 0xFF20 9000 | Out |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

HPS peripherals are mapped to HPS base address space 0xFC00 0000 with 64KB size.

Registers of GPIO0 controller are mapped to the base address 0xFF20 8000 - 0xFF20 8FFF (4KB size)

Registers of GPIO1 controller are mapped to the base address 0xFF20 9000 - 0xFF20 9FFF (4KB size)

Registers of GPIO2 controller are mapped to the base address 0xFF20 A000 - 0xFF20 8FFF (4KB size)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | http://www.altera.com/literature/hb/cyclone-v/cv\_5v4.pdf |  |  |
| GPIO0 | 0xFF20 8000 - 0xFF20 8FFF | 0xFF70 8000 |  |  |
| GPIO1 | 0xFF20 9000 - 0xFF20 9FFF | 0xFF70 9000 |  |  |
| GPIO2 | 0xFF20 A000 - 0xFF20 8FFF | 0xFF70 A000 |  |  |
| LWFPGASLAVES |  | 0xFF20 0000 |  |  |
|  |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |
| gpio0 | 0xFF70 8000 | HPS\_GPIO0\_ADDRESS | HPS\_GPIO0\_OFFSET |  |  |
| gpio\_swporta\_dr | 0 | HPS\_GPIO0\_GPIO\_SWPORTA\_DR\_ADDRESS | GPIO\_GPIO\_SWPORTA\_DR\_OFFSET |  |  |
| gpio\_swporta\_ddr | 0x04 | HPS\_GPIO0\_GPIO\_SWPORTA\_DDR\_ADDRESS | GPIO\_GPIO\_SWPORTA\_DDR\_OFFSET |  |  |
| gpio\_inten | 0x30 | HPS\_GPIO0\_GPIO\_INTEN\_ADDRESS | GPIO\_GPIO\_INTEN\_OFFSET |  |  |
| gpio\_intmask | 0x34 | HPS\_GPIO0\_GPIO\_INTMASK\_ADDRESS | GPIO\_GPIO\_INTMASK\_OFFSET |  |  |
| gpio\_inttype\_level | 0x38 | HPS\_GPIO0\_GPIO\_INTTYPE\_LEVEL\_ADDRESS | GPIO\_GPIO\_INTTYPE\_LEVEL\_OFFSET |  |  |
| gpio\_int\_polarity | 0x3c | HPS\_GPIO0\_GPIO\_INT\_POLARITY\_ADDRESS | GPIO\_GPIO\_INT\_POLARITY\_OFFSET |  |  |
| gpio\_intstatus | 0x40 | HPS\_GPIO0\_GPIO\_INTSTATUS\_ADDRESS | GPIO\_GPIO\_INTSTATUS\_OFFSET |  |  |
| gpio\_raw\_intstatus | 0x44 | HPS\_GPIO0\_GPIO\_RAW\_INTSTATUS\_ADDRESS | GPIO\_GPIO\_RAW\_INTSTATUS\_OFFSET |  |  |
| gpio\_debounce | 0x48 | HPS\_GPIO0\_GPIO\_DEBOUNCE\_ADDRESS | GPIO\_GPIO\_DEBOUNCE\_OFFSET |  |  |
| gpio\_porta\_eoi | 0x4c | HPS\_GPIO0\_GPIO\_PORTA\_EOI\_ADDRESS | GPIO\_GPIO\_PORTA\_EOI\_OFFSET |  |  |
| gpio\_ext\_porta | 0x50 | HPS\_GPIO0\_GPIO\_EXT\_PORTA\_ADDRESS | GPIO\_GPIO\_EXT\_PORTA\_OFFSET |  |  |
| gpio\_ls\_sync | 0x60 | HPS\_GPIO0\_GPIO\_LS\_SYNC\_ADDRESS | GPIO\_GPIO\_LS\_SYNC\_OFFSET |  |  |
| gpio\_id\_code | 0x64 | HPS\_GPIO0\_GPIO\_ID\_CODE\_ADDRESS | GPIO\_GPIO\_ID\_CODE\_OFFSET |  |  |
| gpio\_ver\_id\_code | 0x6c | HPS\_GPIO0\_GPIO\_VER\_ID\_CODE\_ADDRESS | GPIO\_GPIO\_VER\_ID\_CODE\_OFFSET |  |  |
| gpio\_config\_reg2 | 0x70 | HPS\_GPIO0\_GPIO\_CONFIG\_REG2\_ADDRESS | GPIO\_GPIO\_CONFIG\_REG2\_OFFSET |  |  |
| gpio\_config\_reg1 | 0x74 | HPS\_GPIO0\_GPIO\_CONFIG\_REG1\_ADDRESS | GPIO\_GPIO\_CONFIG\_REG1\_OFFSET |  |  |
|  |  |  |  |  |  |

#### Library installation

C:\altera\13.1\embedded\ip\altera\hps\altera\_hps\hwlib

HERE

#### Reference files

|  |  |  |
| --- | --- | --- |
| hps.h |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
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|  |  |  |
|  |  |  |

##### Titre5

###### Titre6

Titre7

Titre8

Titre9

References

* Altera, Cyclone V Devices documentation,  
  <http://www.altera.com/literature/lit-cyclone-v.jsp?ln=devices_fpga&l3=Low-Cost%20FPGAs-Cyclone%20V%20%28E,%20GX,%20GT,%20SE,%20SX,%20ST%29&l4=Documentation>
* Cyclone V Device Handbook Volume 3: Hard Processor System Technical Reference Manual  
  <http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf>
* Cyclone V Hard Processor System User Guide   
  <http://www.altera.com/literature/hb/cyclone-v/cv_5v4_08.pdf>
* Cyclone V, Device Datasheet   
  <http://www.altera.com/literature/hb/cyclone-v/cv_51002.pdf>
* Cylone V HPS addresses   
  <http://www.altera.com/literature/hb/cyclone-v/hps.html>
* Cyclone V Device Handbook Volume 1: Device Interfaces and Integration  
  <http://www.altera.com/literature/hb/cyclone-v/cyclone5_handbook.pdf>
* Cyclone V, Device Overview  
  <http://www.altera.com/literature/hb/cyclone-v/cv_51001.pdf>
* SoCAL documentation (html), The Altera SoC Abstraction Layer (SoCAL) API Reference Manual  
  <file:///C:/altera/13.1/embedded/ip/altera/hps/altera_hps/doc/socal/html/index.html>
* Altera HWLIB, The Altera HW Manager API Reference Manual  
  <file:///C:/altera/13.1/embedded/ip/altera/hps/altera_hps/doc/hwmgr/html/index.html>
* Cyclone V, A Bare-Metal Debugging using ARM DS-5 Altera Edition  
  <http://www.youtube.com/watch?v=CJ0EHJ9oQ7Y>
* Linux Kernel Debug using ARM DS-5 Altera Edition  
  <http://www.youtube.com/watch?v=QcA39O6ofGw>
* FPGA-adaptive debug on the Altera SoC using ARM DS-5  
  <http://www.youtube.com/watch?v=2NBcUv2TxbI>
* A Look Inside: SoC FPGAs Introduction (Part 1 of 5)  
  <http://www.youtube.com/watch?v=RVM-ESUMOMU> (Part 1 of 5)  
  <http://www.youtube.com/watch?v=Ssxf8ggmQk4> (Part 2 of 5)  
  <http://www.youtube.com/watch?v=cWIaqt2RU84> (Part 3 of 5)  
  <http://www.youtube.com/watch?v=gUE669XKhUY> (Part 4 of 5)  
  <http://www.youtube.com/watch?v=NxZznvf5EKc> (Part 5 of 5)
* DS-5 Altera Edition: Bare-metal Debug and Trace  
  <http://www.youtube.com/watch?v=u_xKybPhcHI>
* OpenCL on FPGAs Accelerating Performance and Design Productivity — Altera   
  <http://www.youtube.com/watch?v=M6vpq6s1h_A>

Summary

[1 Introduction 2](#_Toc398519412)

[2 Terasic DE1-SoC Board 3](#_Toc398519413)

[2.1 Specifications 3](#_Toc398519414)

[2.2 Layout 5](#_Toc398519415)

[3 Cyclone V Overview 6](#_Toc398519416)

[3.1 Introduction to the Cyclone V Hard Processor System 6](#_Toc398519417)

[3.2 Features of the HPS 7](#_Toc398519418)

[3.3 HPS Block Diagram 8](#_Toc398519419)

[4 SoC part test 9](#_Toc398519420)

[4.1 HPS Architecture 9](#_Toc398519421)

[4.2 Hardware development 9](#_Toc398519422)

[4.2.1 Qsys integration 9](#_Toc398519423)

[4.3 Software development 11](#_Toc398519424)

[4.3.1 ARM DS-5 tools 11](#_Toc398519425)

[4.3.2 Hello World on ARM HPS part 11](#_Toc398519426)

[4.3.3 GPIO access 13](#_Toc398519427)

List of Figures

[Fig. 1. Fig style **Error! Bookmark not defined.**](#_Toc384979196)

[Fig. 2. Test program for specific parallel port **Error! Bookmark not defined.**](#_Toc384979197)