SOC-FPGA design

Manual

Course Real Time Embedded Systems

LAP – IC – EPFL

Version 0.0 (Preliminary)

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# Introduction

Development of embedded systems based on chip containing one or more microprocessor and hardcore peripherals well as FPGA part is becoming more and more important. This technology allows the the designer a lot of freedom and powerful capabilities. Classical design as with microcontrollers is emphasized with the full power of the FPGAs.

Mixed design are becoming a reality with evolution for the design of specific accelerator the improve a lot of algorithms as well as specific programmable interface with the external world.

Two main HDL (**H**ardware **D**esign **L**anguage) languages are available for the design of the FPGA part VHDL and Verilog. Some tools allow the automatic translation from C to HDL. New technologies emerge as OpenCL to have compatibility between high level design of software and implementation in the hardware as:

* Compilation for a processor or multicore processors
* Compilation for GPU (Graphical Processing Unit)
* Translation and compilation for FPGA, for the last one, PCIe interface is mandatory or another way of parameters passing between the main mandatory processor and the FPGA part is necessary

*This guide assumes that the users know how to use QuartusII, NIOSII, Qsys and ModelSim-Altera.*

The used board is the DE1-soc from terasic: <http://de1-soc.terasic.com>

# DE1-soc board



1. de1-soc board from terasic

Characteristic of the board:

FPGA Device

* Cyclone V SoC **5CSEMA5F31C6** Device
* Dual-core **ARM Cortex-A9** (HPS)
* **85K** Programmable Logic Elements
* 4’450 Kbits embedded memory
* 6 Fractional PLLs
* Hard Memory Controllers

Configuration and Debug

* Quad Serial Configuration device – **EPCQ256** on FPGA
* On-Board **USB Blaster II** (Normal type B USB connector)

Memory Device

* **64MB** (32Mx16) SDRAM on FPGA
* **1GB** (2x256Mx16) DDR3 SDRAM on HPS
* **Micro SD** Card Socket on HPS

Communication

* Two Port USB 2.0 Host (ULPI interface with USB type A connector)
* USB to UART (micro USB type B connector)
* 10/100/1000 Ethernet
* PS/2 mouse/keyboard
* IR Emitter/Receiver

Connectors

* Two 40-pin Expansion Headers
* One 10-pin ADC Input Header
* One LTC connector (One Serial Peripheral Interface (SPI) Master ,one I2C and one GPIO interface )

Display

* 24-bit VGA DAC

Audio

* 24-bit CODEC, Line-in, line-out, and microphone-in jacks

Video Input

* TV Decoder (NTSC/PAL/SECAM) and TV-in connector

ADC

* Fast throughput rate: 1 MSPS
* Channel number: 8
* Resolution: 12 bits
* Analog input range : 0 ~ 2.5 V or 0 ~ 5V as selected via the RANGE bit in the control registe

Switches, Buttons and Indicators

* 4 User Keys (FPGA x4)
* 10 User switches (FPGA x10)
* 11 User LEDs (FPGA x10 ; HPS x 1)
* HPS Reset Buttons (HPS\_RST\_n and HPS\_WARM\_RST\_n)
* Six 7-segment displays

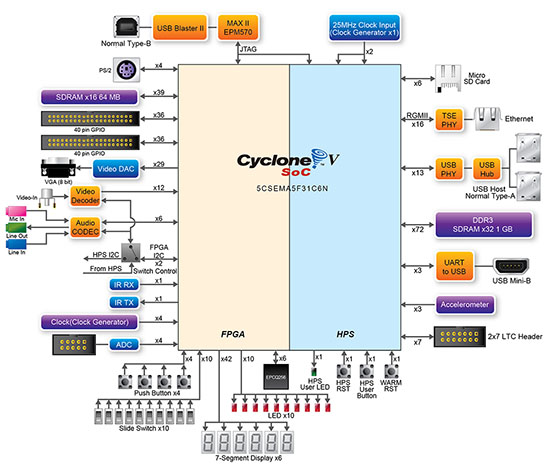
Sensors

* G-Sensor on HPS

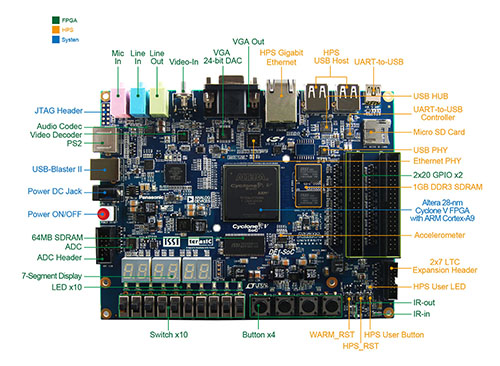
Power

* 12V DC input

Block Diagram of the DE1-SOC Board



1. Block Diagram of the DE1-SOC Board



1. Elements on the de1-soc boards  
   <http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=165&No=836&PartNo=3>

* Green for FPGA part
* Orange for HPS part
* Blue for control

Manuals and resources are available at:

http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=165&No=836&PartNo=4ParagrapheTexte

* Liste

# SOC part test

### ARM DS-5 tools

### Hello World on ARM HPS part

### GPIO access

The references for gpio are:

* <http://www.altera.com/literature/hb/cyclone-v/cv_54022.pdf>
* <http://www.altera.com/literature/hb/cyclone-v/hps.html>
* Supports up to 71 I/O pins and 14 input-only pins depend on device variant

On de1-soc:

* Only 1 Button for HPS GPIO
* Only 1 LED for HPS GPIO

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Pin Name** | **HPS GPIO** | **Register [bit]** | **Function** | **Address** | **Dir** |
| HPS\_KEY | GPIO54 | GPIO1[25] | I/O | 0xFF20 9000 | In |
| HPS\_LED | GPIO53 | GPIO1[24] | I/O | 0xFF20 9000 | Out |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

HPS peripherals are mapped to HPS base address space 0xFC00 0000 with 64KB size.

Registers of GPIO0 controller are mapped to the base address 0xFF20 8000 - 0xFF20 8FFF (4KB size)

Registers of GPIO1 controller are mapped to the base address 0xFF20 9000 - 0xFF20 9FFF (4KB size)

Registers of GPIO2 controller are mapped to the base address 0xFF20 A000 - 0xFF20 8FFF (4KB size)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | http://www.altera.com/literature/hb/cyclone-v/cv\_5v4.pdf |  |  |
| GPIO0 | 0xFF20 8000 - 0xFF20 8FFF | 0xFF70 8000 |  |  |
| GPIO1 | 0xFF20 9000 - 0xFF20 9FFF | 0xFF70 9000 |  |  |
| GPIO2 | 0xFF20 A000 - 0xFF20 8FFF | 0xFF70 A000 |  |  |
| LWFPGASLAVES |  | 0xFF20 0000 |  |  |
|  |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |
| gpio0 | 0xFF70 8000 | HPS\_GPIO0\_ADDRESS | HPS\_GPIO0\_OFFSET |  |  |
| gpio\_swporta\_dr | 0 | HPS\_GPIO0\_GPIO\_SWPORTA\_DR\_ADDRESS | GPIO\_GPIO\_SWPORTA\_DR\_OFFSET |  |  |
| gpio\_swporta\_ddr | 0x04 | HPS\_GPIO0\_GPIO\_SWPORTA\_DDR\_ADDRESS | GPIO\_GPIO\_SWPORTA\_DDR\_OFFSET |  |  |
| gpio\_inten | 0x30 | HPS\_GPIO0\_GPIO\_INTEN\_ADDRESS | GPIO\_GPIO\_INTEN\_OFFSET |  |  |
| gpio\_intmask | 0x34 | HPS\_GPIO0\_GPIO\_INTMASK\_ADDRESS | GPIO\_GPIO\_INTMASK\_OFFSET |  |  |
| gpio\_inttype\_level | 0x38 | HPS\_GPIO0\_GPIO\_INTTYPE\_LEVEL\_ADDRESS | GPIO\_GPIO\_INTTYPE\_LEVEL\_OFFSET |  |  |
| gpio\_int\_polarity | 0x3c | HPS\_GPIO0\_GPIO\_INT\_POLARITY\_ADDRESS | GPIO\_GPIO\_INT\_POLARITY\_OFFSET |  |  |
| gpio\_intstatus | 0x40 | HPS\_GPIO0\_GPIO\_INTSTATUS\_ADDRESS | GPIO\_GPIO\_INTSTATUS\_OFFSET |  |  |
| gpio\_raw\_intstatus | 0x44 | HPS\_GPIO0\_GPIO\_RAW\_INTSTATUS\_ADDRESS | GPIO\_GPIO\_RAW\_INTSTATUS\_OFFSET |  |  |
| gpio\_debounce | 0x48 | HPS\_GPIO0\_GPIO\_DEBOUNCE\_ADDRESS | GPIO\_GPIO\_DEBOUNCE\_OFFSET |  |  |
| gpio\_porta\_eoi | 0x4c | HPS\_GPIO0\_GPIO\_PORTA\_EOI\_ADDRESS | GPIO\_GPIO\_PORTA\_EOI\_OFFSET |  |  |
| gpio\_ext\_porta | 0x50 | HPS\_GPIO0\_GPIO\_EXT\_PORTA\_ADDRESS | GPIO\_GPIO\_EXT\_PORTA\_OFFSET |  |  |
| gpio\_ls\_sync | 0x60 | HPS\_GPIO0\_GPIO\_LS\_SYNC\_ADDRESS | GPIO\_GPIO\_LS\_SYNC\_OFFSET |  |  |
| gpio\_id\_code | 0x64 | HPS\_GPIO0\_GPIO\_ID\_CODE\_ADDRESS | GPIO\_GPIO\_ID\_CODE\_OFFSET |  |  |
| gpio\_ver\_id\_code | 0x6c | HPS\_GPIO0\_GPIO\_VER\_ID\_CODE\_ADDRESS | GPIO\_GPIO\_VER\_ID\_CODE\_OFFSET |  |  |
| gpio\_config\_reg2 | 0x70 | HPS\_GPIO0\_GPIO\_CONFIG\_REG2\_ADDRESS | GPIO\_GPIO\_CONFIG\_REG2\_OFFSET |  |  |
| gpio\_config\_reg1 | 0x74 | HPS\_GPIO0\_GPIO\_CONFIG\_REG1\_ADDRESS | GPIO\_GPIO\_CONFIG\_REG1\_OFFSET |  |  |
|  |  |  |  |  |  |

#### Library installation

C:\altera\13.1\embedded\ip\altera\hps\altera\_hps\hwlib

HERE

#### Reference files

|  |  |  |
| --- | --- | --- |
| hps.h |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

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###### Titre6

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